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A CW Multiplier for High Voltage Generation with A Dc-Dc Converter using Photovoltaic Application

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Abstract— Recent advancements in renewable energy have created a need for both high step-up and high efficiency dc- dc converters. These needs have typically been addressed with converters using high frequency transformers to achieve the desired gain. The transformer design, however, is challenging. This paper presents a high step-up current fed converter based on the classical Cockcroft-Walton (CW) multiplier. The capacitor ladder allows for high voltage gains without a transformer. The cascaded structure limits the voltage stresses in the converter stages, even for high gains. Being current-fed, the converter (unlike traditional CW multipliers) allows the output voltage to be efficiently controlled. In addition, the converter supports multiple input operation without modifying the topology. This makes the converter especially suitable for photovoltaic applications where high gain, high efficiency, small converter size and maximum power point tracking are required. Design equations, a dynamic model, and possible control algorithms are presented. The converter operation was verified using digital simulation and a 450 W prototype converter.

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Keywords: ***CW Multiplier, High Voltage Generation, A Dc-Dc Converter, Photovoltaic Application***

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I. INTRODUCTION

The increased use of photovoltaic (PV) panels for solar power in recent years has led to a great deal of research in dc- dc converter topologies suitable for PV applications. Without a dedicated power converter, the output voltage produced by PV panels is too low to be useful in grid-tied applications. A common solution to this problem involves connecting the panels in a series string configuration. This approach, however, has shortcomings. For instance, both the shading of individual panels in the string and any mismatch between panels affect the power output of every panel in the string. Therefore, connecting a high step-up dc-dc converter to each individual panel is considered a better solution. Doing so allows all panels to produce a maximum amount of power, regardless of the operating state of the other panels in the array.

A large variety of high step-up dc-dc converters exists that would be suitable to use with PV technology. Most of these converters, however, rely on either coupled inductors or high frequency transformers to achieve a high voltage gain. The design of these magnetic components can be complex and time-consuming. Additionally, many topologies require some means of managing component stress to improve efficiency. In most instances, these management techniques require the use of either a soft switching or a Resonant-type converter, further complicating the realization of these converters.

Cascaded converter topologies made from chains of simple basic converters were proposed to reduce the design complex- ity of high step-up dc-dc converters. These types of converters, however, suffer from the fact that, as the number of stages in- creases, the component stresses increase as well. The high component stresses make the practical implementation of these types of converters costly, as components with high voltage ratings are required.

Ladder type, current fed, switched capacitor converters were proposed to address the high component stresses in cascaded converters. The design in uses a Cockcroft-Walton (CW) multiplier fed by a boost converter to achieve high, con- troll able voltage gains. The CW multiplier has the unique characteristic of imposing equal voltage stresses on every stage. Its construction is also simple and easy to implement. The input stage design of is complex because it requires four controllable switches, two of which require high side driving. Although there are off-the-shelf solutions for high-side gate drive, still the complexity and losses of this circuit will be higher than a two-switch topology. Also, the output does not share a return (“ground”) with the input, which necessitates differential voltage sensing and complicates system integra- tion. The topology presented in utilizes a simple boost converter structure at the input, decreasing implementation complexity. However, a different switched capacitor cell is used that greatly reduces the achievable voltage gain. This reduction, in turn, greatly increases the number of components required to realize the desired voltage gain. The topology of achieves a gain similar to the proposed converter andalso supports two input ports, but the inputs and output are all referenced to different returns. The topology of is not amenable to multiple inputs and requires a floating gate driver.

A high gain, current-fed dc-dc converter based on the CW multiplier is presented in Fig. 1. The four switch configuration presented in was replaced by an interleaved boost converteras the input stage. This both reduces the converter's complexity and allows it to perform dual input operation, if desired. The dual input operation enables the controller to operate in three different modes: maximum power point tracking (MPPT) on two separate power sources, power sharing between two power sources while maintaining a controlled output voltage, or inter- leaved operation with a single power source. All three modes of operation are interesting for renewable energy applications. For example, the MPPT on two separate power sources allows one converter to be used with two individual solar panels, increasing the achievable power density and decreasing cost. The interleaved operation from one source is also interesting for MPPT applications, as it features a lower input current ripple than traditional boost converters. This allows more stable operation around the maximum power point of solar panels, decreases the required input capacitance, which in turn reduces cost and size. The power sharing mode with controlled output voltage is interesting in hybrid energy system consisting of a renewable energy sources (such a solar panel or fuel cell) and traditional power sources (like a battery array). The proposed converter can be feed by a renewable energy source on one input and a traditional source on the other. MPPT can then be performed on the renewable energy source, while the remaining energy required to maintain the load is drawn from the stable traditional power source. In addition to the special control modes, the converter features moderate voltage stresses, high gain is achieved with multiple CW stages, and voltage gain on two inputs is adjustable via duty ratio. This makes the converter interesting for any high voltage gain application.

Section II introduces a static model, both ideal and with parasitics, to determine the converter gain and component stresses. Section III derives a linearized dynamic model in state-space form for a 2-stage converter, as an example that may be extended for higher gain converters. Section IV describes two possible control schemes. Section V details the simulation and experimental results that verify the analysis.

II. STEADY STATE ANALYSIS

A. Basic operation

The converter's operation can be separated into four distinct operation modes. Fig. 2 illustrates the current flow pattern during each mode. Fig. 3 illustrates key voltage and current waveforms. Although Fig. 3 implies that d1 = d2, symmetry is not required in actual operation.

Mode 1: The cycle begins when Q2 turns on (treated here as t = 0). Both switches (Q1 and Q2) are conducting. Both inductor currents are increasing. All diodes are reverse-biased.The load is supplied by the output capacitor (Cout).

Mode 2: Switch Q1 is turned off at t = (d1− 0.5)T , which makes the duty ratio of Q1 equal to d1. The current in L1 continues to flow in the diode-capacitor ladder and forward- biases the odd-numbered diodes. The odd-numbered capacitors are all connected in series and discharge into the output capacitor and the even-numbered

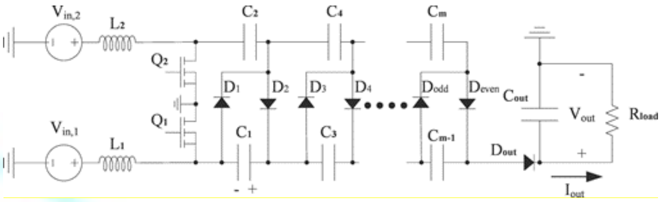
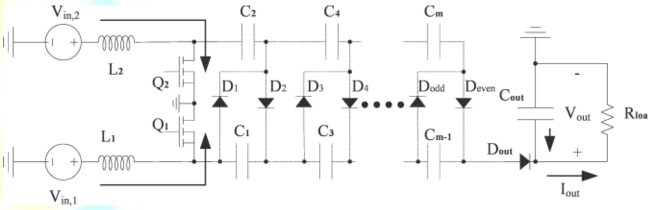
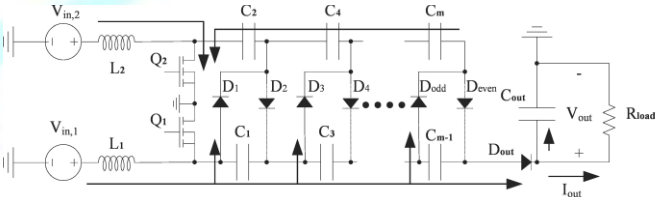


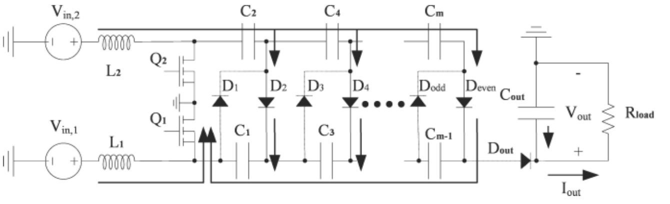
Fig. 1. Current-fed Cockcroft-Walton multiplier



a) Modes 1 & 3



b) Mode 2



c) Mode 4

d) Fig. 2. Current flow patterns in the different operating modes capacitors, which charge. As the capacitor voltages change, diodes become reverse-biased sequentially.

Mode 3: Switch Q1 is turned on at the midpoint of the

cycle, t = 0.5T . Behavior is the same as mode 1.

Mode 4: Switch Q2 is turned off at t = d2T , which makes the duty ratio of Q2 equal to d2. The current in L2 continues to flow and forward-biases the even-numbered diodes. The output diode and odd-numbered diodes remain reverse-biased. The even-numbered capacitors discharge and the odd-numbered capacitors charge. As in mode 2, diodes turn off sequentially as the capacitor voltages change and reverse-bias them. The load is supplied by the output capacitor.

B. Derivation of ideal static gain

The converter in Fig. 1 consists of two building blocks: an interleaved boost converter and a CW multiplier. Also, there are two (slightly asymmetric) halves of the converter. Throughout this work, the two halves will be indexed by

n∈ { 1, 2} where doing so increases clarity; for example, dn will be used where the same equation applies to d1 and d2. The ideal output voltages of the boost converters are

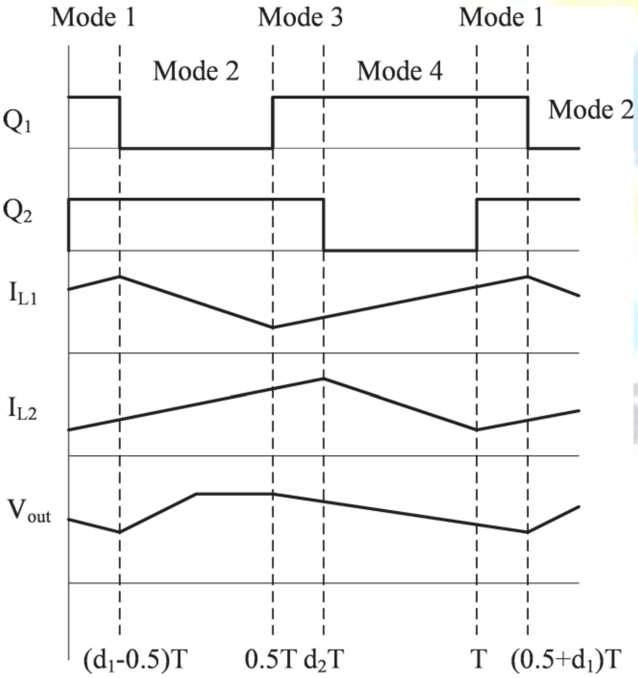


Fig. 3. Key waveforms of the converter.

The CW bridge acts as an ideal transformer for these voltages,so that the ideal output voltage is

$$Vout,target = (1 + N)Vb1 + NVb2 \qquad (2)$$

with N being the total number of stages in the Cockcroft- Walton multiplier and $100\% \geq d_1 + d_2$(One "stage" is defined as two capacitors and two diodes that are coupled, such as C_1, C_2, D_1, and D_2 in Fig. 1.) At least one MOSFET must be on at all times to insure the CW multiplier always has connectionto ground. Therefore, the combined duty ratio of the boost converter switches has to be greater than 100% and the two switching functions must be interleaved so that they overlap. The converter's gain can be adjusted by changing either of theswitch duty ratios.

Power converters are often operated in a symmetrical mode. In the presented converter, both switches can be operated with the same duty ratio (greater than 50%), with the Q_2 command signal delayed by 180°. Also, although the converter supports dual inputs, a single source could be used, $V_{in} = V_{in,1} = V_{in,2}$. This will simplify the equations describing the gain of the converter. The voltage gain for the converter in a symmetrical operation mode is given by $2N + 1$

$$V_{out,tar\,get} = \frac{}{1 - d} V_i \qquad (3)$$

C. Component voltage stresses

Components with both the appropriate voltage and current Equation (2) can be used to calculate these voltage stresses. These, however, only describe the steady-state stress; they do not consider the switching overshoot. Appropriate margins of safety must be applied in accordance with the MOSFET manufacturer specifications.

The maximum voltage stress over the individual stage component is the same as the stage voltage calculated in the ideal voltage derivation. Each stage capacitor and diode must have a rated operating voltage of at least

$$Vstress,stage = Vb1 + Vb2 \qquad (4)$$

The only exceptions to (4) are C2 and the first diode in the ladder, D1, which must only block Vb1.

Under normal operating conditions, the steady-state voltage stress of the output diode is also equal to Vb1. If the converter is connected to a dc bus with a fixed voltage, as in grid-tie solar energy systems, the output diode still needs to be rated for the full output voltage. This will protect the converter from excessive voltage levels when it is not operational or during start-up.

D. Component current stresses

The current stresses for all components need to be determined to aid the designer in selecting the most appropriate components. The peak, average, and RMS currents are of interest to the designer when selecting components with the appropriate rating. These values can also be used in both efficiency calculations and thermal design.

The average currents through the converter's components can be derived from the charge transfers described in a CW. multiplier. The charge supplied by the converter to the output can only travel through the stage diodes in the converter [16]. Therefore, the average current through all diodes in the converter is equal to the converter output current [16]. The average current through the stage capacitors can be determined using the charge each capacitor must transfer each cycle. This will yield the following average capacitor current equation:

$$I_{Cap,m} = 2(N + 1 - m)I_{out} \quad (5)$$

where m is the index of the stage component. The average currents through the boost inductors can be found using conservation of charge: N + 1

$$I_{L1} = \frac{I_{out}}{\frac{1-d_1}{N}} \qquad (6)$$

$$I_{L2} = \frac{I_{out}}{1-d_1} \qquad (7)$$

Similarly, the average currents through the primary switches can be determined using the follo1wing equations:

A digital simulation was also created in Simulink R with PLEC to verify the presented design equations. The parasitic elements such as capacitor ESRs were included in the PLECS model to approximate the experimental system more closely. To verify equation (22) the converter was run with a fixed duty ratio. Both inputs were connected to the same source with a voltage of 25V. The ideal gain for the converter in this configuration is equal to 11.1. Figure 7 shows the predicted value using equation (22), the simulated and experimental results. The difference between the experimental results and voltage predicted by the equation and simulation is due to the non-linearities of the stage diodes [17]. The efficiency of the converter using different duty ratio values is shown in Figure 8.

They impacts the converter's efficiency. Higher current magnitudes in one of the boost inductors (caused by the power sharing) will result in higher RMS currents. These higher RMS currents cause higher losses in the resistive elements of the circuit, reducing the efficiency of the overall converter. Adjusting the duty ratios to ensure equal currents in both boost inductors can increase the efficiency by lowering the RMS currents. However, this operation mode is only an option if both inputs of the converter are connected to the same source.

The control and power sharing capabilities of the converter were verified as well. Figure 9. shows the output voltage and current through the individual loops. Initially the controller is set to command equal current from both loops. At t = 213 s loop 1 was assigned a higher ratio and loop 2 a lower ratio of the required input current. Figure 9 verifies that the output voltage can be maintained when the input current ratio is changed.

The dual MPPT feature was verified using two photovoltaic panels, one connected to each input. The CW multiplier output was connected to a BK8502 electronic load in constant voltage point tracking. At this point panel 2 operates close to its maximum power point. Panel 1 is disconnected from the system, therefore there is a 100% mismatch between panel

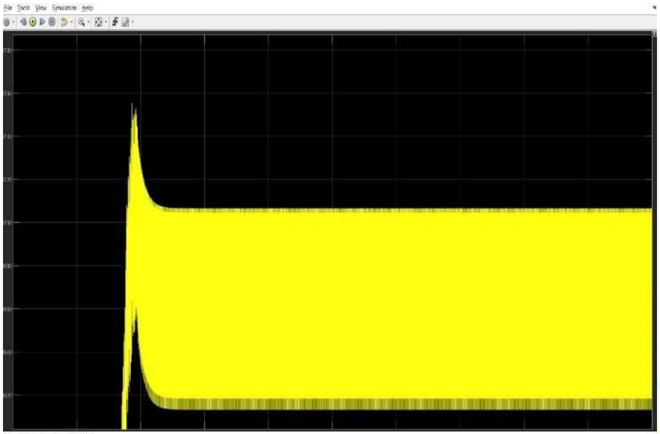
1 and 2. Panel 2 is unable to reach its maximum power point as the duty ratio is close to the maximum value (above 80%). Equation (41) demonstrates the limitations between the allowable duty ratio, input and output voltage. At t = 57 s, panel 1 is connected to CW-multiplier, allowing this panel to supply power as well. Because the system gain changes according to (22), the voltage on panel 2 instantaneously drops. Between t = 57 s and t = 90 s the MPPT algorithm changes the duty ratio of the individual control loops to ensure that both panels operate at their maximum power point (as shown in Fig. 13). After t = 90 s, both panels operate at their maximum power points. Throughout the experiment, the output voltage remains fixed by the electronic load.

This emulates the behavior of a two- stage PV inverter in which the output stage regulates the dc bus voltage by adjusting the power delivered to the grid. The dynamic model was also verified with PLECS simulations. The circuit parameters matched the experimental system, and the load resistance was 500 Ω. The switching frequency was 100 kHz, the input voltages were 30 V and 25 V, and both duty ratios were nominally 0.6. A second Simulink model was constructed from the descriptor state-space model in Section.

The frequency responses were found using the PLECS Multi tone Analysis block, set to apply a multit one sinusoidal perturbation ranging from 100 Hz to 10 kHz to d1 while monitoring the output voltage. The resulting Bode plots are shown superimposed in Fig. 14. The discrepancies at low and high frequencies are artifacts of the per tubation method and the switching nature of the circuit. However, there is excellent agreement at intermediate frequencies. mode to simulate the DC bus in a PV installation. The I-V They impacts the converter's efficiency. Higher current characteristics of the PV panels were measure for the given magnitudes in one of the boost inductors (caused by the power lighting conditions to determine the maximum power point. sharing) will result in higher RMS currents. These higher RMS currents cause higher losses in the resistive elements of the circuit, reducing the efficiency of the overall converter.

Adjusting the duty ratios to ensure equal currents in both boost be seen that panel 2 has a slightly higher maximum power inductors can increase the efficiency by lowering the RMS point than panel 1. The small variations on the panel power currents. However, this operation mode is only an option if both curves is caused by the measurement and quantizing noise of inputs of the converter are connected to the same source.

The results of the MPPT setup are shown in Fig. 12. The duty ratio of both control loops is shown in Fig. 13. Initially both panels were disconnected from the converter, disabling it. At t = 32 s, panel 2 is connected to the current-fed CW multiplier, initializing the maximum power currents cause higher losses in the resistive elements of the circuit, reducing the efficiency of the overall converter. Adjusting the duty ratios to ensure equal currents in both boost inductors can increase the efficiency by lowering the RMS currents. However, this operation mode is only an option if both inputs of the converter are connected to the same source.



III. CONCLUSION

A high gain, current-fed, CW multiplier is presented and analyzed in this paper. The CW multiplier structure limitsthe voltage stresses over the individual stages. This allows components with the same voltage ratings for all of the stage components, regardless of the number of stages or the output voltage of the converter. All equations required to design a practical implementation of the converter are presented in this paper. An equation describing the non-ideal output tage of the converter based on the load, component parameters and duty ratios is given as well. This equation can be used to evaluate the overall performance of the converter and identify the maximum allowable duty ratio range. Additionally, converter control was discussed in this paper. Peak or average current mode control are the most suitable control strategies for the presented topology as the purpose of the input inductors is to act as a current source. The configura-tion of the Cockcroft-Walton multiplier also allows for a dual input operation mode. In this mode the ratio of current between them.

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