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A Comprehensive Review of MOSFET Device Scaling Challenges

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Abstract— the problems with downscaling MOS devices are briefly discussed in this study. Scaling problems like gate oxide tunneling, high electric field, power supply and threshold voltage scaling, hot carrier degradation, random doping fluctuation, parasitic resistance and capacitance, and short channel effect should be thoroughly understood in order to maintain improvement in device density. To maintain the high-density pace, the microelectronics industry may need to move away from conventional MOSFET-based standards and toward those based on molecular nanostructure devices.

Keywords: ***Scaling, Threshold Voltage, Short channel effect, Nanoelectronics, Tunneling,.***

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I. INTRODUCTION

SCALING of CMOS technology has been a fundamental element of the semiconductor industry's current advancement in silicon-based devices. Since a few decades ago, Moore's Law has provided straightforward guidelines for transistor design in order to maximize circuit density and speed. More complex functionality is made possible by the enhanced circuit performance and density since more transistors may be put onto a single chip. However, it turns out that the historical growth, doubling circuit density, and improved performance predicted by Moore's Law cannot be sustained merely by the conventional scaling hypothesis as device scaling continues into the twenty-first century. Further threshold voltage decrease is not possible with increasing leakage current, which in turn prevents supply voltage scaling for speed increase. Leakage currents get worse and device reliability gets poorer when more electric fields are created inside the transistor. Additionally, the necessary high channel doping creates substantial difficulties such mobility deterioration and threshold voltage variations caused by random dopants [1].

1. SIGNIFICANT DOWNSCALING ISSUES IN MOS DEVICES

In order to achieve improved device performances, MOSFET-based CMOS technology must overcome difficulties, namely those related to low power consumption and high ON-state current. The MOS transistor's size is reduced to produce the increased performance. The size of MOSFETs is decreasing from the submicron to the nano scale range. However, the dramatic dimension reduction raises issues that have not yet been resolved and may not always be compatible with device performance.

2. THRESHOLD VOLTAGE AND POWER SUPPLY

To maintain the electric field and active power within bounds, the MOSFET channel down-scaling typically involves a corresponding reduction in supply voltage. The threshold voltage, however, cannot be significantly reduced. This is owing to the fact that a sizeable amount of the total power dissipation in high performance CMOS products is passive power (caused by transistor off-state leakage). Leakage current through the device is the main cause of the power consumption in this condition. In order to prevent a sharp spike in IOFF, VT scaling has therefore slowed down. In order to generate a big drive current, the gate overdrive (VDD - VT) must be considerable, which slows down VDD scaling and increases active power density [3].

3. HIGH ELECTRIC FIELDS

As stated previously, the supply voltage cannot be decreased proportionally to the length of the channel, hence scaling will increase the electric field strength across the gate oxide. Higher vertical electric fields in the MOSFET channel reduce carrier mobilities, which, in the worst-case scenario, can lead to barrier failure and increased leakage currents that can damage the device.

But as transistor device length is continuously reduced that is of SCEs [10-13]. High-K dielectric material is having the capacity of better gate controllability which further makes it as a best gifted device for the low power applications. HfO2 provide large amount of drain current (ID) and it is chosen for dropping the substrate bias effect.

The results of increase in ION/IOFF ratio and transconductance over drain current (gm/ID) will be improved due to high-K dielectric material HfO2 over the device channel [14]. The device is simulated considering the field dependent mobility in addition to velocity saturation which results with many advantages over SiO2.

4. GATE OXIDE TUNNELING

As the electron thermal voltage, kT/q, is constant at room temperature, the ratio between the operational voltage and the thermal voltage decreases as the MOSFET is scaled down. This results in increased leakage currents caused by the thermal diffusion of electrons. With a decrease in channel length, the oxide thickness must likewise decrease proportionally. Quantum mechanical tunneling produces a gate leakage current that grows exponentially with decreasing oxide thickness in thin oxide films. By substituting the oxide gate dielectric with a high-permittivity (high-k) gate dielectric, more scaling can be achieved.

5. PARASITIC RESISTANCES AND CAPACITANCES

As transistors size is decreased, the parasitic resistances and capacitances scale negatively with device area reduction. Consequently, the influence of parasitic components on on-current (ION) increases expressively. These parasitic elements will reduce the performance advantage from scaling transistors.

6. HOT-CARRIER

When charge carriers have high energies and an effective temperature that is larger than the lattice temperature, they are considered as hot carriers. Because they cannot transmit their energy to the lattice atoms quickly enough, these carriers are not in thermal equilibrium with the lattice. They are produced in the inverted channel region when the MOSFET is in linear or saturation mode. The primary issues caused by hot carriers include parasitic gate currents, degradation of drain current, a drop in transconductance, and a shift in threshold voltage with time. The use of a graded drain profile decreases the production of hot carriers [4].

7. RANDOMNESS OF DOPANT DISTRIBUTION

The effect of randomness of dopant distribution on the MOSFET characteristics becomes more risky in small transistor devices, because accurate position of the individual dopant atoms cannot be managed properly. As the device dimensions decrease, it becomes increasingly difficult to put the dopant atoms in the accurate places needed.

8. SOURCE TO DRAIN TUNNELING

If the channel length between source and drain of a MOS device becomes small enough for electrons to tunnel through the device barrier without the gate voltage bias, it can no longer be operated as a switch. Scaling a device should be performed with adequate dimension constraints for proper behavior [7].

9. HEAT DISSIPATION

MOS devices discharge their energy as heat in their resistive components. If this heat is not effectively distributed, the hot spots form on the circuit, causing the material to overheat and the device to breakdown.

10. INTERCONNECT DELAYS

Reducing the wire's width increases its resistance and, thus, increases the delay. This decreases the device speed, and as a result, the device may not be able to operate much faster due to the interconnect delays. Scaling not only aims to enhance device density on chip, but also its speed [6].

11. SHORT-CHANNEL EFFECT (SCES)

As the channel length approaches the depletion depth of the source substrate or drain substrate, the total quantity of depletion charge in the substrate falls. This leads to a decrease in threshold voltage [4]. Particular when the length of a MOSFET channel equals the depth of the source/drain junction and the width of the depletion layer, the device is referred to as a "short channel" rather than a "long channel" in MOSFET devices.

II. CONCLUSIONS

As the scaling of devices approaches their physical size limits, numerous studies have been conducted to find a new solution to sustain Moore's law. Increasing power consumption, process variance, and fabrication costs are decelerating the technological development cycle. Today's device scaling involves tradeoffs between performance and power consumption; hence, technical advancements that enable high performance with very low power consumption are necessary. Even if certain attempts are made to preserve the advanced CMOS technology, its lifespan cannot exceed a few decades. Therefore, developing technologies should be addressed in order to accommodate technological advancements in the near and far future.

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