Optimization of the Radix 4 and Radix 8 Booth Algorithms and Their FPGA Realization

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Abstract— the multipliers play a vital role in performance of any electronics system. But the major drawback is it consumes more power and area. There are numerous methods and techniques available to improve performance while reducing power and space usage. The primary goal of any algorithm for multiplying numbers is to reduce the partial product summation. The booth method is one of the most popular and successful algorithms. In this paper, we propose and implement the booth algorithms for radix 4 and radix 8. In the multiplier encoding, the partial products of the radix 4 algorithm are reduced to n/2, while the partial products of the radix 8 algorithm can be reduced to n/3. The Xilinx Vivado tool is used to produce the simulation results.

Keywords: *Booth algorithm; Booth multiplier; encoding;*

I. INTRODUCTION

HIGH performance processors are in high demand in today's industrial market. Arithmetic operations such as addition, multiplication, and subtraction are invoked in many digital circuits to improve processing speed [1-3]. The multiplier is the slowest part in the system, and its performance determines system performance. The multiplier also takes up a lot of space and has a lot of power dissipation, which affects the overall performance of the system. Multipliers are employed in a variety of applications, including digital signal processing, loss applications, artificial neural networks, machine learning, and many more [4-6].

We have several power reduction methods and multipliers to improve the multiplier's performance. Booth algorithm requires reduced processing time, less design space, and consumes extremely little power. However, the main issue is that the delay is greater. The multiplication operation consists of two major phases, which are as follows:

a. Partial products addition

b. Partial products generation

Multiplier speed can be enhanced by reducing partial products and increasing the speed of partial product summation [7-9].

We will provide optimized radix 4 and radix 8 booth methods for arithmetic operations in this research article.

II. BOOTH ALGORITHM

The booth algorithm was developed by Andrew Donald Booth in year of 1950 at Birkbeck College in Bloomsbury, London. This algorithm was an investigation of computer architecture. Using the 2's complement notation, this booth algorithm multiplies two signed binary values. This algorithm was created while conducting crystallographic research. Less additions and subtraction can be seen in the booth algorithm. The Booth multiplier is the multiplier that does calculations more quickly [10–12]. ASIC products frequently use this booth algorithm because of its small size and quick processing time.

There are three main steps in the booth algorithm:

a. Summation of partial products

b. Reduction of partial products

c. Generation of partial products

The production of partial products in the booth algorithm depends on the recoding process. The procedure makes use of the Booths recoding technique, which is based on the idea that partial products can be produced for a collection of 0s and 1s.

Recoding algorithms' primary goal is to provide effective Partial products. Usually, the Radix utilized for recoding determines whether there will be an increase in partial product [13–15]. Less power and space are provided by this recoding process.
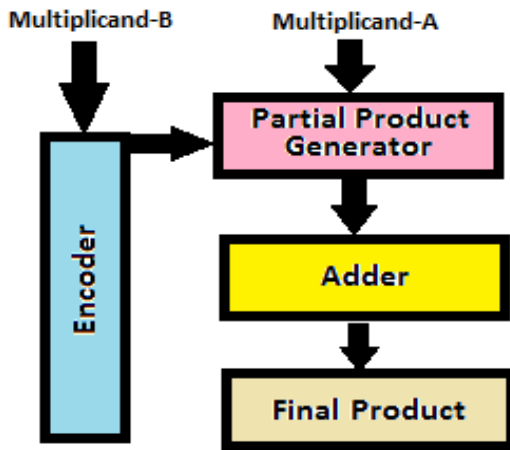
Fig. 1 illustrates the booth algorithm's block diagram, which multiplies two signed binary values in the form of a 2's complement.

We have four blocks in this algorithm, and they function as follows:

i. Encoder:

A digital circuit encoder executes a decoder's opposite operation. It features n outputs and 2n inputs. Here, we have used the encoder's multiplicand B as the input to the booth algorithm, and the encoder's partial product generator as the output. The encoder's output is a binary representation of the input value, and vice versa.

ii. Partially Product Generator:

The partial product generator's primary goal is to make multiplication computations simpler. A group of 0s and 1s can yield the partial products. The speed of the summing of partial products is improved by the partial product reduction.

iii. Adder:

The next phase is summarizing partial products after producing and reducing partial products. To complete this step, we can employ a carry save adder or a carry look ahead adder. There are numerous additional alternatives, including parallel pre-fix adders like the Kogge Stone Adder, Wallace tree adders, compressor adders, and more. We can lower the delay parameter by carefully selecting an adder.

iv. Final product:

The output will be the multiplied 2's compliment number from the inputs multiplicand A and multiplicand B, which can be viewed as two signed binary values.

(i) RADIX 4:

The multiplicands in radix 4 recoding are based on multiplier bits, and it compares three bits at a time using an overlapping process. The grouping will then begin from the LSB bit. Radix 4's primary benefit is its n/2 reduction in the number of partial products.

The steps for radix 4 are as follows:

a. Add 0 to the right of the LSB bit as the first step.

b. We can extend the sign bit 1 place when n is even.

c. The partial products are drawn from the set (-2, 2, 0, 1,-1) where each vector's value is contained.

Y(i+1)	Y(i)	Y(i-1)	Mi	Operation on X
0	0	0	0	0X
0	0	1	+1	+1X
0	1	0	+1	+1X
0	1	1	+2	+2X
1	0	0	-2	-2X
1	0	1	-1	-1X
1	1	0	-1	-1X
1	1	1	0	0X

Table 1: Booth Algorithm Radix 4 truth table

The booth encoding table for the Radix 4 booth algorithm is shown in Table 1. For an example, an 8X8 bit radix 4 considering signed bit as 0 and x as input data of 8-bit ; y as input data of 8-bit and k as the output data , x=11111111 y= 11111111 then k = 1111111000000001

(ii) RADIX 8:

The only difference between radix 8 booth recoding and radix 4 booth recoding is that we examine quartets of bits rather than triplets. In contrast to Radix 4, which decreases the number of partial products to n/2, Radix 8 reduces the number of partial products to n/3. This decrease in Partial products results in faster computations with less power and space consumption.

The booth encoding table for the Radix 8 booth algorithm is shown in Table 2.

Multiplier Bits				Operation on Multiplicand
A	B	C	D	X
0	0	0	0	0X
0	0	0	1	+1X
0	0	1	0	+1X
0	0	1	1	+2X
0	1	0	0	+2X
0	1	0	1	+3X
0	1	1	0	+3X
0	1	1	1	+4X
1	0	0	0	-4X
1	0	0	1	-3X
1	0	1	0	-3X
1	0	1	1	-2X
1	1	0	0	-2X
1	1	0	1	-1X
1	1	1	0	-1X
1	1	1	1	0X

Table 2: Booth Algorithm Radix 8 truth table

For an example , an 8X8 bit radix 8 considering the signed bit as 1 and x as input data of 8-bit ; y as input data of 8-bit and k as the output data , x=11111111 y= 11111111 then k = 1111111111111111.

III. EXPERIMENTAL OBSERVATIONS

The investigational observations were carried out on Xilinx Vivado simulator. Verilog was used to write the HDL code, and vivado was used to display the results of the simulation. The Radix 4 and Radix 8 Booth algorithms' technology schematic, RTL schematic, and wave shapes are displayed here. As opposed to the radix 8 Booth method, which reduces the partial products by n/3 times, radix 4 reduces its partial products to half, or n/2 times.

(i). Booth algorithm Radix 4 results

(a) RTL schematic:

Figure 3 shows the RTL schematic of booth algorithm radix 4, where it provides the information regarding digital logic design in the form of symbols like multipliers, adders etc.
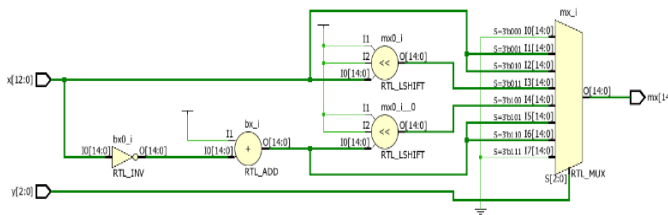
Fig 3: The RTL Schematic of booth algorithm Radix 4
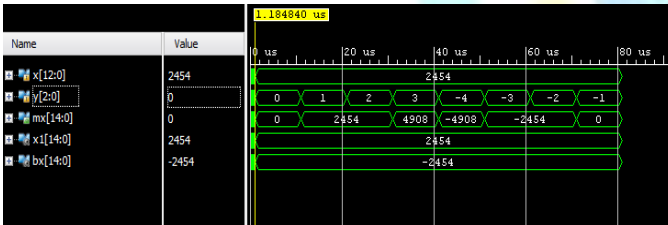
(b) Simulation Timing Diagram

Fig 4: Simulation Timing Diagram of Booth algorithm Radix 4

In this case, the input values for x and y is 12 bits each and has a range of 0 to 7; m is the output value. For instance, when y = 0 and 1 and x = 100110010110 (2454), the output m value remains the same, or "0." The operation is +1x for y = 1 and 2, resulting in m = 2454 as the output value. The procedure is +2x for y=3, resulting in a value of m = 4908.

(i). Booth algorithm Radix 8 results

(a) RTL schematic:

Figure 5 shows the RTL schematic of booth algorithm radix 8, where it provides the information regarding digital logic design in the form of symbols like multipliers, adders etc.

In this case, the output is "m" and the inputs "x" and "y" are each 4 bits wide and range from 0 to 15. If the input values are x = 10011001 (-103) and y = 111 (7), the operation is +4x, and the result is m = 412. The simulation results of the radix 8 booth algorithm are depicted in Figure 7, where X and Y are the input multiplicands and m is the output. As can be seen, two signed binary values are multiplied in the form of their twos complements.
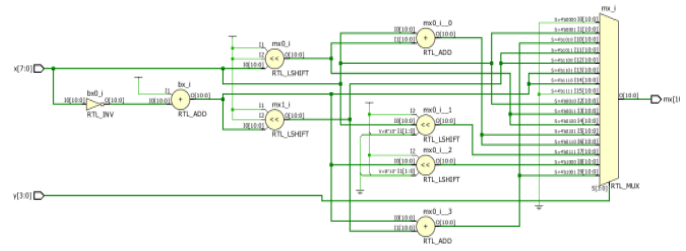
Fig 5: The RTL Schematic of booth algorithm Radix 8
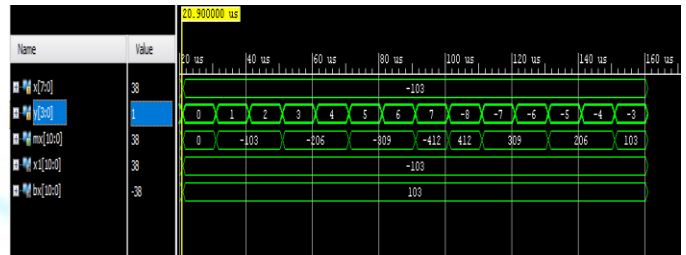
(b) Simulation Timing Diagram

Fig 6: Simulation Timing Diagram of Booth algorithm Radix 8

IV. CONCLUSIONS

The main key parameters for every electronics system are performance and speed. Many low power techniques are being investigated these days to improve performance. The multiplier determines system performance; however the main disadvantage is that it consumes more power and area to improve multiplier performance. Booth algorithm is one of numerous algorithms and types of multipliers accessible. The Booth multiplier have the advantage of having a very high computational speed, which improves the system's performance and speed. We used Xilinx Vivado simulator to implement the Booth algorithms for Radix 4 and Radix 8. We concluded that the Booth algorithm Radix 8 uses less quantity of partial products than Radix 4. As a result, if we design a multiplier employing the booth techniques for radix 8, we can expect very fast computing speed and low power dissipation.

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