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Switching State Step up Converter Mixed with Magnetic Coupling and Voltage Multiplier Techniques for High Gain Conversion

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Abstract— An asymmetrical three state switching step up converter combining the benefits of magnetic coupling and voltage multiplier techniques is presented in this paper. The derivation procedure for the proposed topology is depicted. The new converter can achieve very high voltage gain and very low voltage stress on the power devices without high turn ratio and extreme duty cycles. Thus, the low voltage rated MOSFETs with low resistance can be selected to reduce the switching losses and cost. Moreover, the usage of voltage multiplier technique not only raises the voltage gain but also offers lossless passive clamp performance, so the voltage spikes across the main switches are alleviated and the leakage-inductor energy of the coupled-inductors can be recycled; Also, the interleaved structure is employed in the input side, which not only reduces the current stress through each power switch, but also constrains the input current ripple. In addition, the reverse-recovery problem of the diodes is alleviated, and the efficiency can be further improved. The operating principles and the steady-state analysis of the presented converter are discussed in detail. Finally, a prototype circuit with 400W nominal rating is implemented in the laboratory to verify the performance of the proposed converter.

Keywords: ***Three state switching, high gain, step up converter, magnetic coupling voltage multiplier.***

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I. INTRODUCTION

The high step-up voltage gain dc-dc converters are widely used as an interface between the available low voltage sources and the output loads which are operated at much higher voltage of such applications include high intensity discharge lamp for automotives, DC back-up energy systems for uninterruptible power supplies (UPS), fuel-cell energy-conversion systems, photovoltaic generation systems, telecom back-up facilities, electric vehicles and fuel cell vehicles in above industrial applications, the high step-up dc-dc converters can be non-isolated but they should be operated at high efficiency while taking high currents from low-voltage dc sources at their inputs. Generally, the classical step up is a popular choice for non-isolated applications because of a simple structure and a continuous input current. However, it will be operated at extreme duty cycle, and the rectifier diode must sustain a short pulse current with high amplitude when an extreme high-voltage gain is required. This leads to severe reverse recovery and the electromagnetic interference (EMI) problems. Moreover, the step up switch has to block a high-output voltage and hence the ON-state resistance, which varies almost proportionally with the square of blocking voltage, will be very high so that low-voltage-rated MOSFETs may not be adopted. For those reasons, it is hard for a basic step up converter to achieve both high voltage conversion ratio and high efficiency at the same time.

Some single-switch high step-up step up converters were recently presented in many literatures. From the references Use of cascade of converters is a feasible method for getting desired voltage gain. In addition, previous single-switch converters with high gain also include quadratic step up type, voltage-lift type , switched capacitor or switchedinductor type, and diode-capacitor voltage-multiplier type . Although these converters can achieve higher voltage gain than basic step up converter, the voltage gain of the converters is determined only by the duty cycle of the active switch.

Thus, these converters must cascade more power stages to obtain higher voltage gain, which will result in the complex circuit and low efficiency. Many Converters have been developed to achieve a high step-up voltage ratio without using extreme duty cycle by using tapped-inductor or coupled-inductor. However, the leakage inductor energy of the coupled inductor may cause higher voltage stress on active switch. For this reason, the converters with an active clamp circuit have also been researched in which the cost and circuit complexity are increased. The step up-flyback converters using the coupled inductor and output stacking techniques are proposed which presents low-voltage stress across the switch, and the leakage inductor energy of the coupled inductor is recycled to the output. But, it must be noted that the single active switch will suffer high current stress during the switch-on period for high step up applications for the converters mentioned above, which is non trivial to get higher power. Therefore, it is a major challenge to operate a single switch step up converter at high efficiency for high step-up voltage gain.

As a prominent solution for high input current applications, some interleaved step up converters based on the three state for non-isolated applications because of a simple structure and a continuous input current. However, it will be operated at extreme duty cycle, and the rectifier diode must sustain a short pulse current with high amplitude when an extreme high-voltage gain is required. This leads to severe reverse recovery and the electromagnetic interference (EMI) problems. Moreover, the step up switch has to block a high-output voltage and hence the ON-state resistance, which varies almost proportionally with the square of blocking voltage, will be very high so that low-voltage-rated MOSFETs may not be adopted. For those reasons, it is hard for a basic step up converter to achieve both high voltage conversion ratio and high efficiency at the same time.

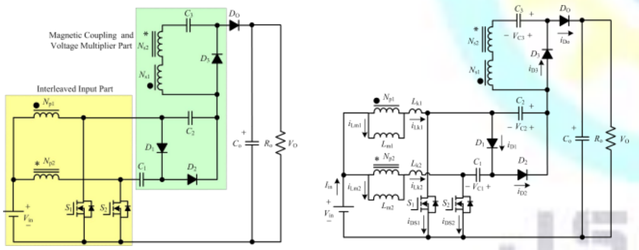

Fig 1: (b) Interleaved step up converter integrating switched capacitors

(c) Circuit configuration of proposed converter

(d) Equivalent circuit of the proposed converter

Fig.1 The procedure to obtain the proposed converter mixed with magnetic coupling and voltage multiplier (c). The secondary windings of two coupled inductors are connected in series for a voltage multiplier rectifier module, which is embedded into above converter. The proposed converter inherits the merits of interleaved technique, switch-capacitor and coupled-inductor techniques, which is suitable for high voltage gain and high power applications. The features of this converter are as follows: this converter can achieve very high voltage gain without extreme duty cycles and high turn ratio. In other words, the turns ratio of the coupled inductor for the presented converter may be designed to be less than its competitions under the same voltage gain and duty ratio; the primary sides of two coupled inductor are used to share the input current by interleaved operation at the input, which reduces the current ripples, the size of magnetic core and the switches conduction loss; Because the diode-capacitor circuit not only raises the step up voltage gain but also offers lossless passive clamp performance, the voltage spikes across the main switches are alleviated and the leakage-inductor energy of the coupled-inductors can be recycled; the voltage stresses on power devices are substantially lower than output voltage. Thus, the switches with low voltage rating and low ON-state resistance RDS (ON) are selected; The current falling rates of the diodes are controlled by the leakage inductance so that the diode reverse-recovery problem is alleviated.

The equivalent circuit of the proposed converter is shown in Fig. 1(d), in which each coupled inductor is modeled as a combination of a magnetizing inductor Lm, an ideal transformer and a leakage inductance Lk (it can be taken as in series to the primary winding), respectively. Moreover, the current through magnetizing inductor Lm is continuous. The coupling references of the inductors are denoted by the marks“*” and “ · ”. The duty cycles of the active switches during steady operation are interleaved with 180°phase shift and greater than 0.5. That is to say, the two switches can only be in one of three states (S1: on, S2: on; S1: on, S2: off; S1: off, S2: on;), whose main objective is to obtain high voltage gain and such characteristic is achieved when the duty cycle is greater than 0.5, hence, the steady-state analysis is made only for this case. It is important to point out that the proposed

A novel three-level inverter has been proposed in this paper for PV applications. This inverter can boost the input photo-voltaic (PV) voltage up to three times in output without additional DC/DC converter. Two switched capacitor (SC) cells are connected in a cascade manner to boost the input PV voltage. Further, this topology can eliminate the leakage current completely, as it bypasses the parasitic capacitance by way of a common ground (CG) connection between the negative terminal of the PV panel and the neutral of the grid. Consequently, it does not need an electro-magnetic interference (EMI) filter for electromagnetic compatibility (EMC). The additional feature of the proposed inverter is reactive power handling capability. A proportional resonant (PR) current controller has been implemented to regulate the active and reactive components of the grid current. The proposed modulation strategy makes the inverter capable of balancing the switched capacitors by charging during its inactive state. The inverter operating principle, operating modes, and modulation scheme have been analyzed in detail. The various claims about the proposed inverter have been verified in MATLABO simulation, and the results are presented.

The features of this converter are as follows: this converter can achieve very high voltage gain without extreme duty cycles and high turn ratio. In other words, the turns ratio of the coupled inductor for the presented converter may be designed to be less than its competitions under the same voltage gain and duty ratio; the primary sides of two coupled inductor are used to share the input current by interleaved operation at the input, which reduces the current ripples, the size of magnetic core and the switches conduction loss; Because the diode-capacitor circuit not only raises the step up voltage gain but also offers lossless passive clamp performance, the voltage spikes across the main switches

A. Coupled Inductor Design

Since the turns ratio determines the voltage gain and voltage stress on the semiconductor devices, it is one of the can be obtained by (21)-(23), respectively. The estimated capacitances are: key parameters for the presented converter. To be clear, the proposed converter can work under different turns ratio for the double coupled inductors, but increase the complexity of circuit analysis and design. Moreover, large turn's ratio difference may cause the raise of input current ripple. So the turns ratio of the coupled inductors will be designed as same as possible in this paper. Usually, the duty cycle should be less than 0.8 to reduce conduction loss of the switches. If the voltage gain and switch duty cycle are selected, the turns ratio of the coupled inductor can be calculated by

$$N = \frac{1}{2}[M \cdot (1-D) - 3] \quad (35).$$

Generally, the equivalent series resistor (ESR) of an aluminum electrolytic capacitor will be smaller as the capacitance increases. So the aluminum electrolytic capacitor is usually selected to be larger than the calculated value for reducing the power losses caused by the ESR, but the large capacitor is bulky volume and high cost. In practice, it is a favorable solution that parallel several capacitors are adopted to make the equivalent ESR minimum. In addition, the film capacitors could be used to improve the efficiency and minimize the capacitances. But, the cost of film capacitors is higher. According to the equation (24), the voltage gain will be less affected by the leakage inductance of the coupled inductors. Fortunately, the leakage inductance can be used to limit the diode current falling rate and alleviate the diode reverse recovery problem. Therefore, a compromise should be made to optimize the performance of the converter. Moreover, considering the input current ripples, the leakage inductance of the coupled inductors should be designed as symmetrical as possible. The relationship of the leakage inductance, the diode current falling rate, and the turns ratio is expressed by equation

$$\frac{di_{D3}}{dt} = \frac{di_{DO}}{dt} \approx \frac{V_{C3}}{N^2(L_{k1}+L_{k2})} \quad (36).$$

B. Active Switches and Diodes Selection

The voltage-rating of the power components have been derived from (25)-(28). In practice, voltage spike may be produced during switch transition process because of the effect of parasitic parameters in the lay-out circuit. Therefore, regarding the margin of safety, the voltage rating of the selected power devices will usually be more than 150% of the calculated value.

C. Considerations of Capacitor Design

The capacitors C1, C2 and C3 play the roles of buffering energy, clamping the voltage stress on the power devices and improving voltage gain. Calculating the minimum capacitance of the switched capacitors depends on the maximum transferring power, the capacitor's voltage, and the switching frequency [42]. The voltage of C1, C2 and C3 can be obtained by (21)-(23), respectively. The estimated capacitances are

$$C_1 \geq \frac{2P_{O\_max}}{V_{C1}^2 f_s}; C_2 \geq \frac{2P_{O\_max}}{V_{C2}^2 f_s}; C_3 \geq \frac{2P_{O\_max}}{V_{C3}^2 f_s} \quad (37)$$

Generally, the equivalent series resistor (ESR) of an aluminum electrolytic capacitor will be smaller as the capacitance increases. So the aluminum electrolytic capacitor is usually selected to be larger than the calculated value for reducing the power losses caused by the ESR, but the large capacitor is bulky volume and high cost. In practice, it is a favorable solution that parallel several capacitors are adopted to make the equivalent ESR minimum. In addition, the film capacitors could be used to improve the efficiency and minimize the capacitances. But, the cost of film capacitors is higher.

II. EXPERIMENTAL VERIFICATIONS

In order to verify the operation and evaluate the performance of the proposed three-state switching step up converter, an experimental prototype for the structure mixed with diode-capacitors and coupled inductors has been designed according to the previous guidelines and implemented in laboratory. The components used in the prototype are listed in Table II.

Table. II Utilized components and parameters of prototype

Components	Parameters
Input voltage V_{in}	16-22V
Output voltage V_o	200V
Maximum output power P	400W
Switching frequency f_s	50kHz
Turns ratio N_s/N_p	1:1
Magnetizing inductor L_{m1},L_{m2}	55uH
Leakage inductor L_{k1},L_{k2}	1.65 uH
Power switches S_1,S_2	FDP2532
Diodes D_1, D_2 and D_3	MUR2020
Diode D_O	MUR2040
Capacitors C_1 and C_2	10uF/100 V
Capacitor C_3	22uF/100 V
Capacitor C_O	470uF/ 200V

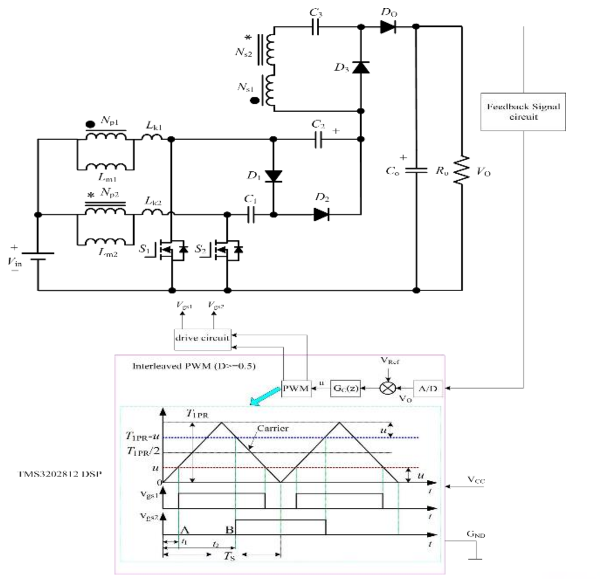

Fig.2 Simple digital control strategy for the proposed converter based on DSP

In control strategy, the proposed converter is controlled by the TMS3202812DSP as shown in Fig. 2.This technique consists in sampling the output voltage and comparing it to a reference, which generates an error voltage. This error serves as a parameter to the compensator, providing the control voltage, which, after the modulation, provides pulse width modulation pulses for driving switches, with adjusted duty cycle for stabling output voltage on the desired level. Fig. 3 (a) presents the behavior of the input current and the currents through the primary side leakage inductance currents iLK1 and iLK2 of the dual coupled inductors, where it can be seen that the currents through Lk1and Lk2 are operated in interleaving. Consequently, the stresses regarding the active switches are reduced and the input current ripples are very low. Fig.3 (b) shows the gate signals of S1 and S2, current waveforms and the voltage stresses passing through them.

One can see that the active switches are turned on from lower current, which reduces the switching losses and the EMI noise. In addition, the voltage stresses Vds1and Vds2 on the main switches are equal, which is one fifth of the output voltage during the steady-state period, about 40 V. Thus low voltage ratings and low on-state resistance levels active switches can be selected for high conversion efficiency.

Fig. 3 (c) displays that the voltage and current stresses on the diodes D1 and D2. One can see that the voltage stresses of the diodes D1, D2 are approximately 80V which are lower than half of the output voltage in the steady-state period. Therefore, low-voltage rated diodes with high performance can be adopted for the presented converter. Moreover, the diodes D1 and D2 are automatically turned off. Fig. 3 (d) illustrates that the voltage and current stresses on the diodes D3 and DO. The voltage stress of the diodes D3 is about 80V, and the voltage stress of the diode DO is approximately 120V which are lower than the output voltage in the steady-state period. In addition, the currents through D3 and DO at the instant of the turning OFF are reduced what favors the turning OFF behavior, which agree converter, and the VC3 is nearly equal to VC1 because the turns ratio N is set 1. The VC2 is about twice of VC1, which is agreement with theoretical analysis. Fig. 13(f) shows the dynamic response due to the step load variation between 200 and 400 W, and the output voltage is maintained at 200

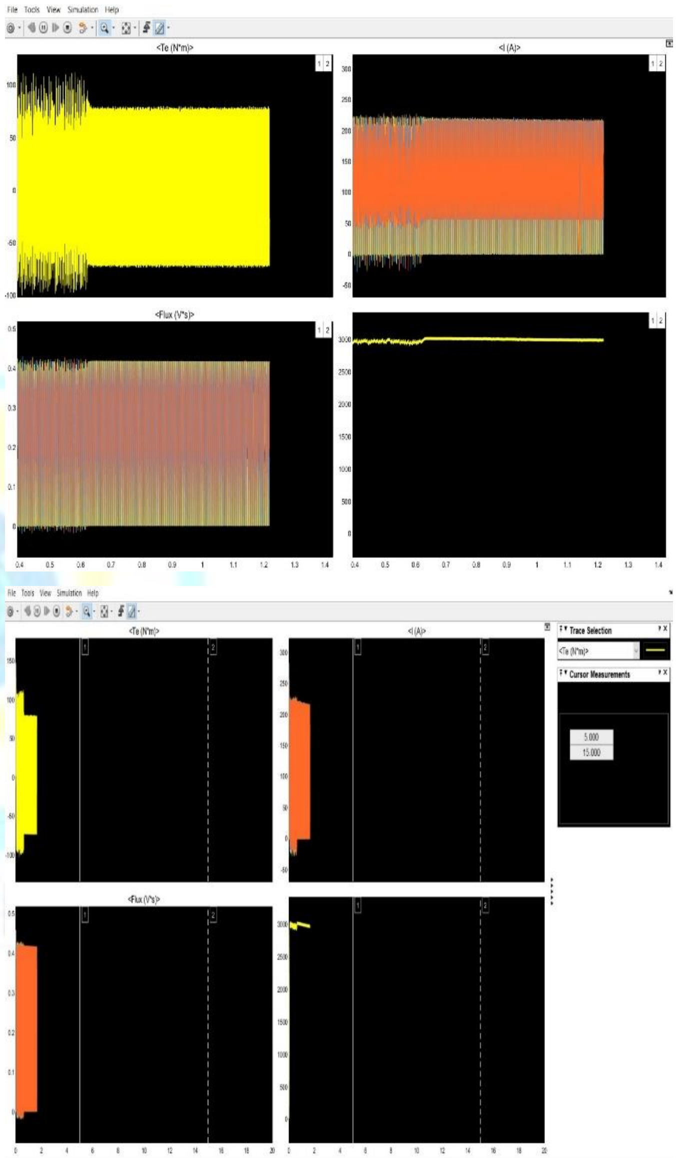

Fig. 3 (e) shows the experimental results of voltage on all capacitor to illustrate the theoretical analysis. The VC1 equal to the output voltage of the conventional step up

III. CONCLUSIONS

In this paper, a three state switching step up converter with high-voltage gain has been successfully developed, which is mixed with magnetic coupling and voltage multiplier techniques, and suitable for low input-voltage and high step up power conversion application Moreover, the generation methodology for the proposed topology is described. The key theoretical waveforms, steady-state operational principle and the main circuit performance are clearly analyzed and verified, exploring the advantages of the proposed converter. The proposed converter can achieve a very high voltage gain and avoid operating at extreme voltage stresses of the main switches are very low, which are one fifth of the output voltage under N=1. Thus, the low-voltage-rated MOSFETs with low resistance rDS(ON) can be selected to reduce the switching losses and cost. Moreover, the interleaved PWM operation reduces the current through each switch and restrains the input current ripples effectively. In addition, the current falling rates of the diodes are controlled by the leakage inductance so that the diode reverse-recovery problem is alleviated, and the leakage inductance energy can be recycled to the output through capacitors C1 and C2; meanwhile, there will be no overshoot current of capacitors C1 and C2 for the existence of leakage inductance. Therefore, the proposed converter is promising for high step up applications. Still, the disadvantage of this topology is that the duty cycle of each switch shall be not less than 0.5 under the interleaved control with 180°phase shift, in order to ensure the normal energy transmission.

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