Journal of Science, Computing and Engineering Research (JSCER)
Volume-7, Issue-10, October 2024.
DOI: *https://doi.org/10.46379/jscer.2023.07100*

An Expert Estimator Tool to check Project Cost and Risk with Early Stage of Function Points

Archana Meena, Umar Qamar Niwaas, R.K Singh

Assistant Professor, Ambalika Institute of Management and Technology , India

Article Information

Received : 02 Oct 2024
Revised : 06 Oct 2024
Accepted : 18 Oct 2024
Published : 22 Oct 2024

Corresponding Author:

Archana Meena

Abstract— This paper presents the comparison of proposed double tail comparator with conventional double tail and existing double tail comparator. The low power and high-speed analog to digital converters used are of dynamic regenerative comparators to maximize speed. Presenting different architectures for calculating delay and power consumption in dynamic double tail comparator. The power gating technique is used to design the proposed comparator. By using this technique, delay and power consumption is reduced compared to the conventional double tail comparator and the existing double tail comparator. The important parameters are speed and power consumption. Cadence design tools used to simulate the comparator in the 90nm technology with the supply voltage of 0.6v.

Keywords: ***Dynamic latch comparator, speed, power consumption, high speed analog to digital converter.***

Citation: Archana Meena, Umar Qamar Niwaas, R.K Singh, "An Expert Estimator Tool to check Project Cost and Risk with Early Stage of Function Points", Journal of Science, Computing and Engineering Research, 7(10), October 2024.

I. INTRODUCTION

Comparator is a circuit that output is binary information depending upon the comparison of two input voltages here the comparison in between analog voltage and reference voltage. Analog voltage is greater than reference voltage, and then comparator output is logic '1'. The comparator output is logic '0', when analog voltage is less than reference voltage. Comparators are effectively used in analog to digital (ADC) converters. In analog to digital conversion process [1], the analog voltage is converted in to samples for getting accuracy. Those samples are given to set of comparators in order to achieve equivalent binary information. The schematic of

. Hence, designing highspeed comparators with low supply voltages many techniques are there such boosting [6] methods, techniques employing body driven comparator circuit works in reset phase. CMOS technology

II. RELATED WORKS

In comparator circuits to reduce power consumption the Power gating technique is proposed. In this technique, circuit operates in sleep mode by switching off the current in circuit. Power gating has the benefit that is it measures current (Idd) in the quiescent state. In this paper the different architectures of double tail comparator is presented. The proposed comparator is designed by using power gating technique. Using this technique power and delay is reduced.

III. BACKGROUND OF STUDY

The circuit diagram of the single tail comparator shown in Fig 3. The single tail comparator circuit operation is given below. When CLK=0 the circuit works in reset phase so the Mtail NMOS transistor is in off position and the reset transistors M7 and M8 PMOS transistors are in on position now the output at OUTN and OUTP will be VDD. When CLK= VDD , Mtail NMOS transistor is in ON position and M7 and M8 PMOS transistors are in OFF position now the OUTN and OUTP urrent to keep the differential amplifiers in weak condition so a large current required enabling fast regeneration in the circuit.

IV. METHODOLOGY

This structure has the power consumption 20.49 nW and circuit delay is 38.83 ps. Circuit diagram of the conventional double tail comparator shown in Fig 4. This structure has low static power consumption and operates at lower supply voltages compare to the single tail comparator. The working of this comparator is given below.

When CLK=0 the to discharge with different charging rates. Due to these

ending on the input voltages INN and INP. When INP voltage>INN voltage, M1 NMOS transistor provides less current than M2 NMOS transistor due to this current fn discharges faster than fp. The disadvantage of this structure is static power consumption whenever the current drawn from VDD to ground through input and Mtail1 transistor. To overcome static power consumption in proposed double tail comparator two NMOS transistors MSW1 and MSW2 used below the input transistor

V. RESULTS AND DISCUSSIONS

All the circuits are designed by using Cadence Virtuoso tool and simulated in 90 nm CMOS technology with the supply voltage of 0.6V. The output waveform of comparator

shown in Fig 8. Power waveform of the single tail comparator is shown in Fig 9.

VI. CONCLUSION

Comparison of three double tail comparator circuits being done. All the circuits simulated by using cadence design tools 90nm technology with the supply voltage of 0.6 volt. Using the power gating technique, power consumption and delay is reduced in the proposed double tail comparator. The proposed double tail comparator consumes less power and delay is also reduced compare to previous comparator circuits. Due to additional NMOS transistors there is an increase in area. The comparator circuit used in analog to digital converter structures, sense amplifier, operational amplifier and pre defined amplifier.

REFERENCES

[1]. P. Nirmala, T. Manimegalai, J. R. Arunkumar, S. Vimala, G. Vinoth Rajkumar, Raja Raju, "A Mechanism for Detecting the Intruder in the Network through a Stacking Dilated CNN Model", Wireless Communications and Mobile Computing, vol. 2022, Article ID 1955009, 13 pages, 2022. https://doi.org/10.1155/2022/1955009.

[2]. D. Sathyanarayanan, T. S. Reddy, A. Sathish, P. Geetha, J. R. Arunkumar and S. P. K. Deepak, "American Sign Language Recognition System for Numerical and Alphabets," 2023 International Conference on Research Methodologies in Knowledge Management, Artificial Intelligence and Telecommunication Engineering (RMKMATE), Chennai, India, 2023, pp. 1-6, doi: 10.1109/RMKMATE59243.2023.10369455.

[3]. J. R. Arunkumar, Tagele berihun Mengist, 2020" Developing Ethiopian Yirgacheffe Coffee Grading Model using a Deep Learning Classifier" International Journal of Innovative Technology and Exploring Engineering (IJITEE) ISSN: 2278-3075, Volume-9 Issue-4, February 2020. DOI: 10.35940/ijitee.D1823.029420.

[4]. Ashwini, S., Arunkumar, J.R., Prabu, R.T. et al. Diagnosis and multi-classification of lung diseases in CXR images using optimized deep convolutional neural network. Soft Comput (2023). https://doi.org/10.1007/s00500-023-09480-3

[5]. J.R.Arunkumar, Dr.E.Muthukumar," A Novel Method to Improve AODV Protocol for WSN" in Journal of Engineering Sciences" ISSN NO: 0377-9254Volume 3, Issue 1, Jul 2012.

[6]. R. K, A. Shameem, P. Biswas, B. T. Geetha, J. R. Arunkumar and P. K. Lakineni, "Supply Chain Management Using Blockchain: Opportunities, Challenges, and Future Directions," 2023 Second International Conference on Informatics (ICI), Noida, India, 2023, pp. 1-6, doi: 10.1109/ICI60088.2023.10421633.

[7]. Arunkumar, J. R. "Study Analysis of Cloud Security Chanllenges and Issues in Cloud Computing Technologies." Journal of Science, Computing and Engineering Research 6.8 (2023): 06-10.

[8]. J. R. Arunkumar, R. Raman, S. Sivakumar and R. Pavithra, "Wearable Devices for Patient Monitoring System using IoT," 2023 8th International Conference on Communication and Electronics Systems (ICCES), Coimbatore, India, 2023, pp. 381-385, doi: 10.1109/ICCES57224.2023.10192741.

[9]. S. Sugumaran, C. Geetha, S. S, P. C. Bharath Kumar, T. D. Subha and J. R. Arunkumar, "Energy Efficient Routing Algorithm with Mobile Sink Assistance in Wireless Sensor Networks," 2023 International Conference on Advances in Computing, Communication and Applied Informatics (ACCAI), Chennai, India, 2023, pp. 1-7, doi: 10.1109/ACCAI58221.2023.10201142.

[10]. R. S. Vignesh, V. Chinnammal, Gururaj.D, A. K. Kumar, K. V. Karthikeyan and J. R. Arunkumar, "Secured Data Access and Control Abilities Management over Cloud Environment using Novel Cryptographic Principles," 2023 International Conference on Advances in Computing, Communication and Applied Informatics (ACCAI), Chennai, India, 2023, pp. 1-8, doi: 10.1109/ACCAI58221.2023.10199616.

[11]. Syamala, M., Anusuya, R., Sonkar, S.K. et al. Big data analytics for dynamic network slicing in 5G and beyond with dynamic user preferences. Opt Quant Electron 56, 61 (2024). https://doi.org/10.1007/s11082-023-05663-2

[12]. Krishna Veni, S. R., and R. Anusuya. "Design and Study Analysis Automated Recognition system of Fake Currency Notes." Journal of Science, Computing and Engineering Research 6.6 (2023): 16-20.

[13]. V. RamKumar, S. Shanthi, K. S. Kumar, S. Kanageswari, S. Mahalakshmi and R. Anusuya, "Internet of Things Assisted Remote Health and Safety Monitoring Scheme Using Intelligent Sensors," 2023 International Conference on Advances in Computing, Communication and Applied Informatics (ACCAI), Chennai, India, 2023, pp. 1-8, doi: 10.1109/ACCAI58221.2023.10199766.

[14]. R. S. Vignesh, R. Sankar, A. Balaji, K. S. Kumar, V. Sharmila Bhargavi and R. Anusuya, "IoT Assisted Drunk and Drive People Identification to Avoid Accidents and Ensure Road Safety Measures," 2023 International Conference on Advances in Computing, Communication and Applied Informatics (ACCAI), Chennai, India, 2023, pp. 1-7, doi: 10.1109/ACCAI58221.2023.10200809.

[15]. I. Chandra, G. Sowmiya, G. Charulatha, S. D, S. Gomathi and R. Anusuya, "An efficient Intelligent Systems for Low-Power Consumption Zigbee-Based Wearable Device for Voice Data Transmission," 2023 International Conference on Artificial Intelligence and Knowledge Discovery in Concurrent Engineering (ICECONF), Chennai, India, 2023, pp. 1-7, doi: 10.1109/ICECONF57129.2023.10083856.

[16]. G. Karthikeyan, D. T. G, R. Anusuya, K. K. G, J. T and R. T. Prabu, "Real-Time Sidewalk Crack Identification and Classification based on Convolutional Neural Network using Thermal Images," 2022 International Conference on Automation, Computing and Renewable Systems (ICACRS), Pudukkottai, India, 2022, pp. 1266-1274, doi: 10.1109/ICACRS55517.2022.10029202.

[17]. R. Meena, T. Kavitha, A. K. S, D. M. Mathew, R. Anusuya and G. Karthik, "Extracting Behavioral Characteristics of College Students Using Data Mining on Big Data," 2023 International Conference on Artificial Intelligence and Knowledge Discovery in Concurrent Engineering

(ICECONF), Chennai, India, 2023, pp. 1-7, doi: 10.1109/ICECONF57129.2023.10084276.

[18]. S. Bharathi, A. Balaji, D. Irene. J, C. Kalaivanan and R. Anusuya, "An Efficient Liver Disease Prediction based on Deep Convolutional Neural Network using Biopsy Images," 2022 3rd International Conference on Smart Electronics and Communication (ICOSEC), Trichy, India, 2022, pp. 1141-1147, doi: 10.1109/ICOSEC54921.2022.9951870.

[19]. I. Chandra, G. Sowmiya, G. Charulatha, S. D, S. Gomathi and R. Anusuya, "An efficient Intelligent Systems for Low-Power Consumption Zigbee-Based Wearable Device for Voice Data Transmission," 2023 International Conference on Artificial Intelligence and Knowledge Discovery in Concurrent Engineering (ICECONF), Chennai, India, 2023, pp. 1-7, doi: 10.1109/ICECONF57129.2023.10083856.

[20]. Revathi, S., et al. "Developing an Infant Monitoring System using IoT (INMOS)." International Scientific Journal of Contemporary Research in Engineering Science and Management 6.1 (2021): 111-115.

[21]. J.R.Arunkumar, Dr.E.Muthukumar,‖ A Novel Method to Improve AODV Protocol for WSN‖ in Journal of Engineering Sciences‖ ISSN NO: 0377-9254Volume 3, Issue 1, Jul 2012.

[22]. R. S. Vignesh, A. Kumar S, T. M. Amirthalakshmi, P. Delphy, J. R. Arunkumar and S. Kamatchi, "An Efficient and Intelligent Systems for Internet of Things Based Health Observance System for Covid 19 Patients," 2023 International Conference on Artificial Intelligence and Knowledge Discovery in Concurrent Engineering (ICECONF), Chennai, India, 2023, pp. 1-8, doi: 10.1109/ICECONF57129.2023.10084066.

[23]. I. Chandra, K. V. Karthikeyan, R. V, S. K, M. Tamilselvi and J. R. Arunkumar, "A Robust and Efficient Computational Offloading and Task Scheduling Model in Mobile Cloud Computing," 2023 International Conference on Artificial Intelligence and Knowledge Discovery in Concurrent Engineering (ICECONF), Chennai, India, 2023, pp. 1-8, doi: 10.1109/ICECONF57129.2023.10084293.

[24]. R. K, A. Shameem, P. Biswas, B. T. Geetha, J. R. Arunkumar and P. K. Lakineni, "Supply Chain Management Using Blockchain: Opportunities, Challenges, and Future Directions," 2023 Second International Conference on Informatics (ICI), Noida, India, 2023, pp. 1-6, doi: 10.1109/ICI60088.2023.10421633.

[25]. J. R. Arunkumar, and R. Anusuya, “OCHRE: A Methodology for the Deployment of Sensor Networks.” American Journal of Computing Research Repository, vol. 3, no. 1 (2015): 5-8.