

A case study of Insurance Companies Quality Leadership Style in Relation to Enterprise Commitment in India

Grihidhar S, Jambulingam S Menon

Assistant Professor, Metha College of Engineering, ECE Dept, Meera, India

Article Information

Received : 02 April 2024
Revised : 06 April 2024
Accepted : 08 April 2024
Published : 10 April 2024

Corresponding Author:

Grihidhar S, Jambulingam S Menon

Abstract— This paper presents the comparison of proposed double tail comparator with conventional double tail and existing double tail comparator. The low power and high-speed analog to digital converters used are of dynamic regenerative comparators to maximize speed. Presenting different architectures for calculating delay and power consumption in dynamic double tail comparator. The power gating technique is used to design the proposed comparator. By using this technique, delay and power consumption is reduced compared to the conventional double tail comparator and the existing double tail comparator. The important parameters are speed and power consumption. Cadence design tools used to simulate the comparator in the 90nm technology with the supply voltage of 0.6v.

Keywords: *Dynamic latch comparator, speed, power consumption, high speed analog to digital converter.*

Copyright © 2024: Grihidhar S, Jambulingam S Menon, This is an open access distribution, and reproduction in any medium, provided Access article distributed under the Creative Commons Attribution License the original work is properly cited License, which permits unrestricted use.

Citation: Grihidhar S, Jambulingam S Menon, “A case study of Insurance Companies Quality Leadership Style in Relation to Enterprise Commitment in India”, Journal of Science, Computing and Engineering Research, 7(3), March 2024.

I. INTRODUCTION

Comparator is a circuit that output is binary information depending upon the comparison of two input voltages here the comparison in between analog voltage and reference voltage. Analog voltage is greater than reference voltage, and then comparator output is logic '1'. The comparator output is logic '0', when analog voltage is less than reference voltage. Comparators are effectively used in analog to digital (ADC) converters. In analog to digital conversion process [1], the analog voltage is converted in to samples for getting accuracy. Those samples are given to set of comparators in order to achieve equivalent binary information. The schematic of a voltage comparator shown in Fig 1. Comparator transfer characteristics shown in Fig 2. Comparator truth table shown in Table 1. Comparator applications are analog to digital converters and data receivers. The dynamic latch comparators used in these applications in order to achieve high-speed and low power. Dynamic comparators have no static power consumption because of strong positive feedback. Dynamic latch comparator [3] is suitable for high-speed analog to digital converters (ADC). The first stage of clocked comparator is given to the inputs. Second stage of clocked comparator consists of two cross coupled inverters called regenerative stage. In this stage each inverter input is connected to the other inverter output. The important parameters like speed, power consumption, and transistor count are very important in comparator applications. By using a clocked regenerative structure will get low power and good output swing. When the clock is high (CLK= VDD) comparator circuit works in comparison phase. When the clock is low (CLK=0)

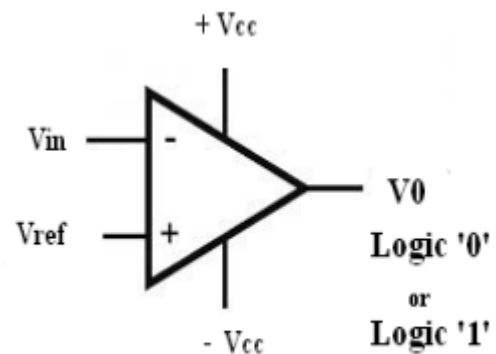


Fig 1. Schematic of comparator

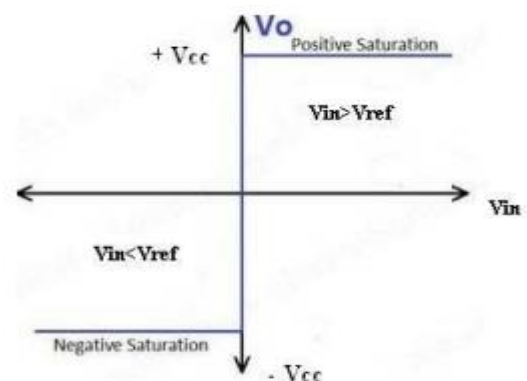


Fig 2. Comparator Transfer Characteristics

TABLE I.
COMPARATOR TRUTH TABLE

| CLK | INN | INP | OUTN | OUTP |
|-----|-----|-----|------|------|
| 0 | X | X | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 |

suffers from low supply voltages for designing high speed comparators. Hence, designing highspeed comparators with low supply voltages many techniques are there such boosting [6] methods, techniques employing body driven comparator circuit works in reset phase. CMOS technology

II. RELATED WORKS

In comparator circuits to reduce power consumption the Power gating technique is proposed. In this technique, circuit operates in sleep mode by switching off the current in circuit. Power gating has the benefit that is it measures current (I_{dd}) in the quiescent state. In this paper the different architectures of double tail comparator is presented. The proposed comparator is designed by using power gating technique. Using this technique power and delay is reduced.

III. BACKGROUND OF STUDY

The circuit diagram of the single tail comparator shown in Fig 3. The single tail comparator circuit operation is given below. When $CLK=0$ the circuit works in reset phase so the M_{tail} NMOS transistor is in off position and the reset transistors $M7$ and $M8$ PMOS transistors are in on position now the output at $OUTN$ and $OUTP$ will be V_{DD} . When $CLK=V_{DD}$, M_{tail} NMOS transistor is in ON position and $M7$ and $M8$ PMOS transistors are in OFF position now the $OUTN$ and $OUTP$ output nodes are discharge depending on the INN and INP input voltages. When $INP > INN$, $M5$ PMOS transistor will turn ON because of $OUTP$ discharges more speed than $OUTN$ then the output at $OUTN=V_{DD}$ and output at $OUTP=0$. When $INP < INN$ voltage, drain current of the transistor $M2$ causes faster discharge of $OUTP$ compared to $OUTN$. Advantages of the single tail comparator are high input impedance, output swing without noise, no static power consumption. The disadvantage is only one current path is available via M_{tail} NMOS transistor which defines the current for both the differential amplifiers that means a small tail current to keep the differential amplifiers in weak condition so a large current required enabling fast regeneration in the circuit.

IV. METHODOLOGY

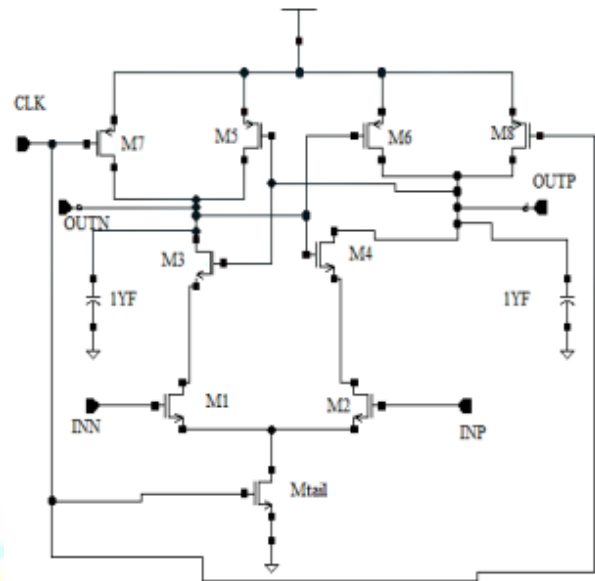


Fig 3. Circuit diagram of the single tail comparator

This structure has the power consumption 20.49 nW and circuit delay is 38.83 ps. Circuit diagram of the conventional double tail comparator shown in Fig 4. This structure has low static power consumption and operates at lower supply voltages compare to the single tail comparator. The working of this comparator is given below.

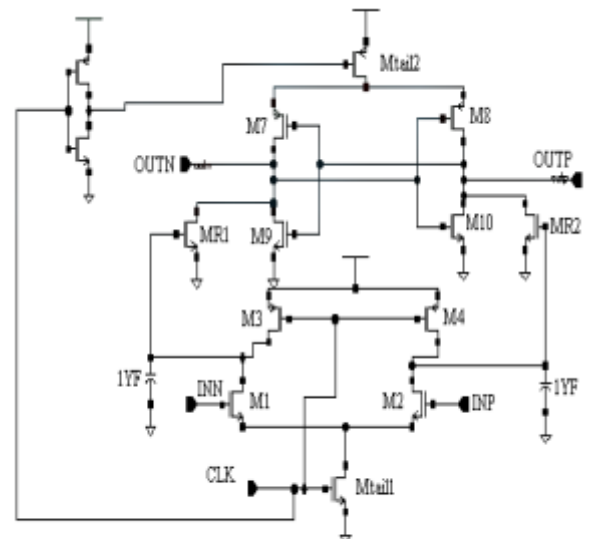


Fig 4. Circuit diagram of conventional Double tail comparator

When $CLK=0$ the circuit works in reset phase so the M_{tail1} NMOS transistor and M_{tail2} PMOS transistor are in OFF position and the $M3$ and $M4$ PMOS transistors will turn on then the value at nodes fn and $fp=V_{DD}$ due to this V_{DD} , $MR1$ and $MR2$ turn ON and discharge the output nodes $OUTP$ and $OUTN$ to the ground. When $CLK=V_{DD}$,

the circuit works in comparison phase resulting in Mtail1 NMOS transistor and Mtail2 PMOS transistor to switch ON. The M3 and M4 PMOS transistors will turn OFF then the voltages at nodes fn and fp starts to discharge with different charging rates. Due to these discharging transistors MR1 and MR2 are in OFF position so they do not play any role in improving the transconductance. The circuit power consumption and delay is 59.06 nW and 80.09 ns respectively. The IV section explains how the existing comparator improves performance of double tail comparator.

Circuit diagram of the existing double tail comparator with static power consumption shown in Fig 5. The existing comparator designed for low voltage applications based on conventional double tail comparator. The main idea of this comparator is to increase V_{fn}/V_{fp} ratio and speed up the latch regenerative circuit. MC1 and MC2 PMOS transistors are connected in parallel to M3 and M4 PMOS transistors. This set up is used to increase speed of the existing comparator. Power consumption of this comparator is 3.468 uW and over all delay is 20.31 ns. The schematic of existing double tail comparator without static power consumption shown in Fig 6. The working of proposed double tail comparator is given below.

When CLK=0 the circuit works in reset phase, Mtail1 NMOS transistor and Mtail2 PMOS transistor are in OFF position and the M3 and M4 PMOS transistors will turn ON then the value at nodes fn and fp= VDD, hence MC1 and MC2 PMOS transistors are OFF. Intermediate stage transistors MR1 and MR2 will turn ON because of the value at nodes fn and fp= VDD. Consequently the value at OUTN and OUTP=0. When CLK=VDD the circuit works in comparison phase so the Mtail1 NMOS transistor and Mtail2 PMOS transistor is in ON position and the transistors M3 and M4 are in OFF state, nodes fn and fp start to discharge at different charging rates depending on the input voltages INN and INP. When INP voltage > INN voltage, M1 NMOS transistor provides less current than M2 NMOS transistor due to this current fn discharges faster than fp. The disadvantage of this structure is static power consumption whenever the current drawn from VDD to ground through input and Mtail1 transistor. To overcome static power consumption in proposed double tail comparator two NMOS transistors MSW1 and MSW2 used below the input transistor

V. RESULTS AND DISCUSSIONS

All the circuits are designed by using Cadence Virtuoso tool and simulated in 90 nm CMOS technology with the supply voltage of 0.6V. The output waveform of comparator shown in Fig 8. Power waveform of the single tail comparator is shown in Fig 9. Conventional double tail comparator's power waveform shown in Fig 10. Power waveforms of the existing double tail with static power and without static power are shown in Fig 11 and Fig 12 respectively. Power waveform of the proposed double tail

comparator shown in Fig13. Power comparison and delay comparison shown in Table 2 and Table 3 respectively. From this analysis known that the proposed double tail comparator consumed less power and delay also reduced compare to existing and conventional double tail comparator.

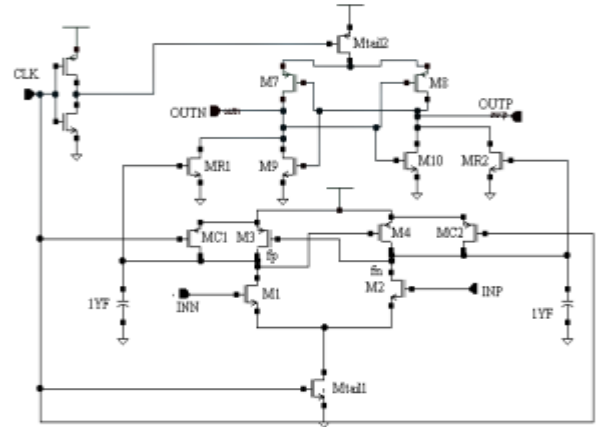


Fig 5. Schematic of the existing Double tail comparator with static power consumption

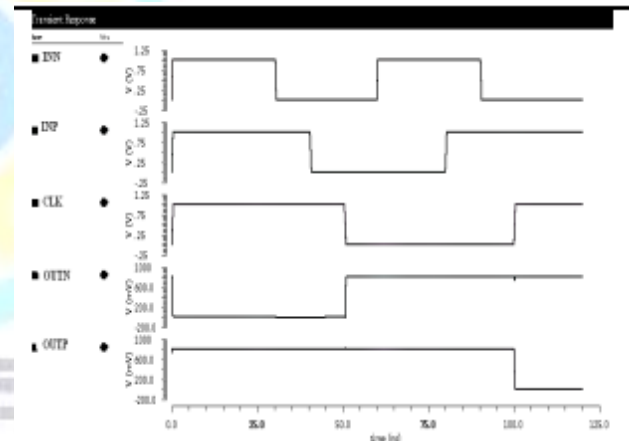


Fig 8. Output waveform of comparator

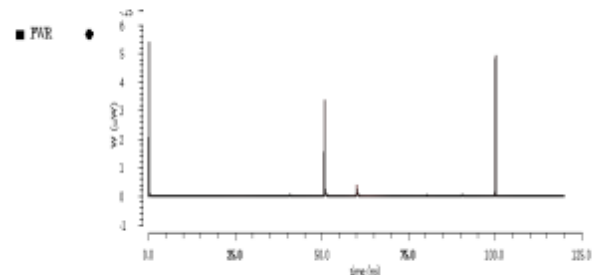


Fig 9. Power waveform of the single tail comparator

VI. CONCLUSION

Comparison of three double tail comparator circuits being done. All the circuits simulated by using cadence design

tools 90nm technology with the supply voltage of 0.6 volt. Using the power gating technique, power consumption and delay is reduced in the proposed double tail comparator. The proposed double tail comparator consumes less power and delay is also reduced compare to previous comparator circuits. Due to additional NMOS transistors there is an increase in area. The comparator circuit used in analog to digital converter structures, sense amplifier, operational amplifier and pre defined amplifier.

REFERENCES

- [1]. P. Nirmala, T. Manimegalai, J. R. Arunkumar, S. Vimala, G. Vinoth Rajkumar, Raja Raju, "A Mechanism for Detecting the Intruder in the Network through a Stacking Dilated CNN Model", *Wireless Communications and Mobile Computing*, vol. 2022, Article ID 1955009, 13 pages, 2022. <https://doi.org/10.1155/2022/1955009>.
- [2]. D. Sathyanarayanan, T. S. Reddy, A. Sathish, P. Geetha, J. R. Arunkumar and S. P. K. Deepak, "American Sign Language Recognition System for Numerical and Alphabets," 2023 International Conference on Research Methodologies in Knowledge Management, Artificial Intelligence and Telecommunication Engineering (RMKMATE), Chennai, India, 2023, pp. 1-6, doi: 10.1109/RMKMATE59243.2023.10369455.
- [3]. J. R. Arunkumar, Tagele berihun Mengist, 2020" Developing Ethiopian Yirgacheffe Coffee Grading Model using a Deep Learning Classifier" International Journal of Innovative Technology and Exploring Engineering (IJITEE) ISSN: 2278-3075, Volume-9 Issue-4, February 2020. DOI: 10.35940/ijitee.D1823.029420.
- [4]. Ashwini, S., Arunkumar, J.R., Prabu, R.T. et al. Diagnosis and multi-classification of lung diseases in CXR images using optimized deep convolutional neural network. *Soft Comput* (2023). <https://doi.org/10.1007/s00500-023-09480-3>
- [5]. J.R.Arunkumar, Dr.E.Muthukumar," A Novel Method to Improve AODV Protocol for WSN" in *Journal of Engineering Sciences* ISSN NO: 0377-9254 Volume 3, Issue 1, Jul 2012.
- [6]. R. K, A. Shameem, P. Biswas, B. T. Geetha, J. R. Arunkumar and P. K. Lakineni, "Supply Chain Management Using Blockchain: Opportunities, Challenges, and Future Directions," 2023 Second International Conference on Informatics (ICI), Noida, India, 2023, pp. 1-6, doi: 10.1109/ICI60088.2023.10421633.
- [7]. Arunkumar, J. R. "Study Analysis of Cloud Security Challenges and Issues in Cloud Computing Technologies." *Journal of Science, Computing and Engineering Research* 6.8 (2023): 06-10.
- [8]. J. R. Arunkumar, R. Raman, S. Sivakumar and R. Pavithra, "Wearable Devices for Patient Monitoring System using IoT," 2023 8th International Conference on Communication and Electronics Systems (ICES), Coimbatore, India, 2023, pp. 381-385, doi: 10.1109/ICES57224.2023.10192741.
- [9]. S. Sugumaran, C. Geetha, S. S, P. C. Bharath Kumar, T. D. Subha and J. R. Arunkumar, "Energy Efficient Routing Algorithm with Mobile Sink Assistance in Wireless Sensor Networks," 2023 International Conference on Advances in Computing, Communication and Applied Informatics (ACCAI), Chennai, India, 2023, pp. 1-7, doi: 10.1109/ACCAI58221.2023.10201142.
- [10]. R. S. Vignesh, V. Chinnammal, Gururaj.D, A. K. Kumar, K. V. Karthikeyan and J. R. Arunkumar, "Secured Data Access and Control Abilities Management over Cloud Environment using Novel Cryptographic Principles," 2023 International Conference on Advances in Computing, Communication and Applied Informatics (ACCAI), Chennai, India, 2023, pp. 1-8, doi: 10.1109/ACCAI58221.2023.10199616.
- [11]. Syamala, M., Anusuya, R., Sonkar, S.K. et al. Big data analytics for dynamic network slicing in 5G and beyond with dynamic user preferences. *Opt Quant Electron* 56, 61 (2024). <https://doi.org/10.1007/s11082-023-05663-2>
- [12]. Krishna Veni, S. R., and R. Anusuya. "Design and Study Analysis Automated Recognition system of Fake Currency Notes." *Journal of Science, Computing and Engineering Research* 6.6 (2023): 16-20.
- [13]. V. RamKumar, S. Shanthi, K. S. Kumar, S. Kanageswari, S. Mahalakshmi and R. Anusuya, "Internet of Things Assisted Remote Health and Safety Monitoring Scheme Using Intelligent Sensors," 2023 International Conference on Advances in Computing, Communication and Applied Informatics (ACCAI), Chennai, India, 2023, pp. 1-8, doi: 10.1109/ACCAI58221.2023.10199766.
- [14]. R. S. Vignesh, R. Sankar, A. Balaji, K. S. Kumar, V. Sharmila Bhargavi and R. Anusuya, "IoT Assisted Drunk and Drive People Identification to Avoid Accidents and Ensure Road Safety Measures," 2023 International Conference on Advances in Computing, Communication and Applied Informatics (ACCAI), Chennai, India, 2023, pp. 1-7, doi: 10.1109/ACCAI58221.2023.10200809.
- [15]. I. Chandra, G. Sowmiya, G. Charulatha, S. D, S. Gomathi and R. Anusuya, "An efficient Intelligent Systems for Low-Power Consumption Zigbee-Based Wearable Device for Voice Data Transmission," 2023 International Conference on Artificial Intelligence and Knowledge Discovery in Concurrent Engineering (ICECONF), Chennai, India, 2023, pp. 1-7, doi: 10.1109/ICECONF57129.2023.10083856.
- [16]. G. Karthikeyan, D. T. G, R. Anusuya, K. K. G, J. T and R. T. Prabu, "Real-Time Sidewalk Crack Identification and Classification based on Convolutional Neural Network using Thermal Images," 2022 International Conference on Automation, Computing and Renewable Systems (ICACRS), Pudukkottai, India, 2022, pp. 1266-1274, doi: 10.1109/ICACRS55517.2022.10029202.
- [17]. R. Meena, T. Kavitha, A. K. S, D. M. Mathew, R. Anusuya and G. Karthik, "Extracting Behavioral Characteristics of College Students Using Data Mining on Big Data," 2023 International Conference on Artificial Intelligence and Knowledge Discovery in Concurrent Engineering (ICECONF), Chennai, India, 2023, pp. 1-7, doi: 10.1109/ICECONF57129.2023.10084276.
- [18]. S. Bharathi, A. Balaji, D. Irene, J. C. Kalaivanan and R. Anusuya, "An Efficient Liver Disease Prediction based on Deep Convolutional Neural Network using Biopsy Images," 2022 3rd International Conference on Smart Electronics and Communication (ICOSEC), Trichy, India, 2022, pp. 1141-1147, doi: 10.1109/ICOSEC54921.2022.9951870.
- [19]. I. Chandra, G. Sowmiya, G. Charulatha, S. D, S. Gomathi and R. Anusuya, "An efficient Intelligent Systems for Low-Power Consumption Zigbee-Based Wearable Device for Voice Data Transmission," 2023 International Conference on Artificial Intelligence and Knowledge Discovery in Concurrent Engineering (ICECONF), Chennai, India, 2023, pp. 1-7, doi: 10.1109/ICECONF57129.2023.10083856.

Intelligence and Knowledge Discovery in Concurrent Engineering (ICECONF), Chennai, India, 2023, pp. 1-7, doi: 10.1109/ICECONF57129.2023.10083856.

- [20].Revathi, S., et al. "Developing an Infant Monitoring System using IoT (INMOS)." International Scientific Journal of Contemporary Research in Engineering Science and Management 6.1 (2021): 111-115.

