Journal of Science, Computing and Engineering Research (JSCER)
Volume-7, Issue- 3, March 2024.
DOI: *https://doi.org/10.46379/jscer.2023.070304*

Depressed Power Utilization on 3T Gain Cell EDRAMerence Mitigation in Cognitive for Femtocell Networks

G. Sruthi Rani, V. Hemalaxmi, B. Srikalanithi

Assistant Professor,Princeton College of Engineering & Tech, Hyderabad, India

Article Information

Received : 02 March 2024

Revised : 06 March 2024

Accepted : 08 March 2024

Published : 10 March 2024

Corresponding Author:

G. Mehalatha

Abstract— Logic compatible gain cell (GC)-embedded DRAM (eDRAM) arrays are considered an alternative to SRAM because of their small size, non rationed operation, low static leakage, and two-port functionality. But traditional GC-eDRAM implementations require boosted control signals in order to write full voltage levels to the cell to reduce the refresh rate and shorten access times. The boosted levels require an extra power supply or on-chip charge pumps, as well as nontrivial level shifting and toleration of high voltage levels. In this paper, we present a novel, logic compatible, 3T GC-eDRAM bit cell that operates with a single-supply voltage and provides superior write capability to the conventional GC structures. The proposed circuit is demonstrated in 0.25µm CMOS process targeted at low power, energy efficient application.

Keywords: **DRAM, GC, VLSI, SRAM, 3T, Cell.**

Copyright © 2024:, G. Sruthi Rani, V. Hemalaxmi, B. Srikalanithi, This is an open access distribution, and reproduction in any medium, provided Access article distributed under the Creative Commons Attribution License the original work is properly cited License, which permits unrestricted use.

Citation: G. Sruthi Rani, V. Hemalaxmi, B. Srikalanithi, "Depressed Power Utilization on 3T Gain Cell EDRAMerence Mitigation in Cognitive for Femtocell Networks", Journal of Science, Computing and Engineering Research, 7(3), March 2024.

I. INTRODUCTION

Memories have occupied large proportion of the die area of VLSI system-on chips in recent years. Major reason for this is increasing number of components as in case of 6T SRAM it has large 6-transistor the various other reasons are area- consuming, peripheral circuitry. Embedded memories have turned to be an important one in the long standby mode it continues to leak more power which characterize the system performance.

Initially SRSAMs are used for storing data bits in memory. But it has some of the disadvantages like large area, more power consumption even though it has been the traditional choice for the implementation of embedded memories due to its high-access speed and refresh-free data retention time. It also has some other disadvantages like static leakage of current, under voltage scaling and large transistor count. These limitations can be overcome by usage of gain- cell (GC)-embedded DRAM (eDRAM) such as circuit in Fig.

2 and Fig. 3 [3]-[8]. Which provides full CMOS logic compatibility of 2-transistor (2T) or 2-transistor (3T) GC-eDRAMS resulting in nonratioed operation and low static leakage currents from VDD to GND. Inspite of overcoming most of the disadvantages of static memories GC-eDRAM requires periodic refreshing operation. However, as opposed to static memories the data retention time of GC-eDRAM depend on dynamically stored charge.

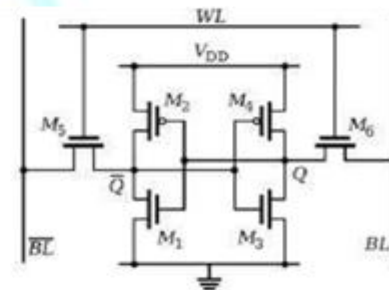

Fig.1 6T SRAM

Basic static RAM circuits can be viewed as vibrations on the designs used for latches and flip-flops more aggressive static RAMs make use of design tricks originally developed RAMs to speed up the system. The value is stored in the middle four transistors, of Fig.1 which form a pair on inverters connected in a loop. The other two transistors control access to the memory cell by the bit lines. When select = 0, the inverters reinforce each other to store the value. A read or write is performed when cell is selected.

To read, bit and bit are pre charged to before the select line is allowed to go high. One of the cell's inverters will have its output at 1, and the other at 0, which inverter is 1 depends on the value stored. The right hand inverter's pull down and the bit line will be drained to through that inverter's pull down and the bit line will remain high. If the opposite value is stored in the cell, the bit lines will be pulled own while bit remains high. To write, the bit and bit lines are set to the desired value, then select is set to 1.charge sharing forces the inverters to switch values, if necessary, to store the desired value. The bit lines have much higher capacitance than

B. 2T Mixed Gain Cell

2T mixed GC can be implemented with either an NMOS or a PMOS device as shown in Fig.2. Moreover, both MW (write transistor) and MR (read transistor) can be implemented with standard threshold voltage core or high threshold voltage I/O devices in the considered CMOS technology. Due to the voltage drop across MW, a boosted write word line (WWL)voltage is required during write access above for NMOS operation and below for PMOS operation. conducting and charges RBL post a detectable sensing threshold. If SN holds value MR is cut-off such that RBL remains discharged below the sensing threshold. For the NMOS implementation of MR, the operation is exactly opposite i.e. RBL is precharged and RWL is lowered to initiate a read.

II. PROPOSED METHOD

In this brief, we present a new topology for a 3TGC, featuring a complementary transmission gate in the write port. While the proposed solution is quite straight forward it is novel and its impact in very high. We demonstrate the functionality of the proposed system used in ultra-low power applications such as biomedical sensor nodes and implants. The proposed 3T GC-eDRAM macro is shown to be fully functional with a supply voltage ranging from 600mv to 2.5v.

3T GC consists of write port featuring a complementary transmission gate PMOS write (PW) and NMOS write (NW) a storage node (SN) composed of the three transistors, a read port based on NMOS read (NR) and the metal interconnect as in Fig 3. the GC is built that all the transistors operates with standard voltage and is fully compatible with standard digital CMOS technologies. The gates of PW and NW are connected to the world line of PMOS and NMOS WWLp and WWLn. A common write bit line is used to drive the data to the

transmission gate during write operations. When the full- swing is given to the cells transmission gate enables the propagation of strong levels to the SN without any need for boosted world line. RBL capacitances or blocking the discharge path if SN is low. IN order to achieve a tradeoff between speed, area, power and reliability, a dynamic sense amplifier can be used to improve the read operation and its performance as described in [5],[6].

III. OPERATIONS

The circuit is described with = 900 mv. This voltage was chosen as a good medium voltage between and since the data retention time (DRT) is proved to be efficient in. GC-eDRAM design [8] at this voltage starting with charged WBL is driven low and the world lines WWLp is set to 0 and WWLn is set to . Then a strong 0 level is passed to the SN, during standby, the level on SN deteriorates due to leakage currents dominated by the sub threshold leakage of PW and NW in mature CMOS nodes. Hence in order to extend the retention time WBL is driven to during standby and read cycles thereby significantly reducing the sub threshold leakage through the transmission gate for both stored low and high values compared with the condition where WBL is either driven to either or GND. The write circuitry and read circuitry are described in section IV.A. During readout the 0 level blocks the discharge paththrough NR, maintaining the precharged voltage on RBL. During the next write operation WBL is driven high, resulting in a strong1 stored on the SN. The subsequent read operation provides a strong gate overdrive to transistor NR, thereby discharging RBL toread a 1. It should be noted that during this operation (Read 1), bitcells storing 1 and sharing thesame column turn on when RBL discharges by more than the of NR, causing it to saturate before it can completely discharge. This phenomenon is common to many GC-eDRAM configurations, as discussed in[8].

IV. DATA RETENTION TIME

The data retention time (DRT) of GC embedded DRAMS is the time interval for writing a data level in the bit cell to the last moment the data can still correctly read out the stored information. For 2T and 3T cells methodology which are affected by the initially degraded voltage level corresponding to the data values due to the threshold voltage () drop across the write transistor DRT is primarily limited by the initial charge stored on the internal bit cell capacitance and the leakage currents that degrade the stored voltage level over time. In order to describe this issue a boosted write world line (WWL) voltage is usually employed to pass a full swing level to the storage capacitance. Any how this requires the generation of boosted on-chip voltage, which entails substantial overhead [1]. The magnitude of the voltage boost is set not only to overcome the drop, but also to achieve short write access time which otherwise are typically longer than 6T SRAM implementation. The proposed bitcells provides strong initial data levels for enhanced DRT and robust operation as well as for fast write access time.

V. MACRO PERIPHERALS

To improve the array performance in terms of access time and power consumption several peripheral techniques were integrated into the designed memory macro in the proposed technique single supply voltage is provided to the circuit which simplifies the implementation of a full memory macro. This is the significant advantage over the other GC eDRAMS that uses conventional bit cells. These bit cells require the use of level shifters to create the desired boosted or negative voltage supply depending on the types of MOS write. The

peripheral circuit which is designed for this memory macro and their techniques are described as follows.

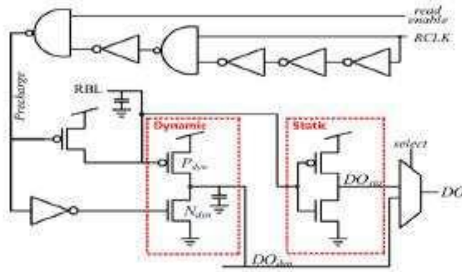

Fig.4.ReadOut Circuitry

VI. READOUT CIRCUITRY

Large number of ultra low power systems comprising of low voltage embedded memories consists of simple sense inverter. This sense inverter is used for the purpose of reduction in area, robust and low power readout operation however this inverter suffers from very slow data readout as it requires RBL to be discharged or charged for PMOS read device switching the threshold of the inverter.

GC-eDRAM macro cell has two sensing node 1). A faster dynamic sensing mode but it is potentially more error-phrone which acts in dynamic readout mode 2). A slightly slower static mode but more reliable. In both the sensing modes however threshold device PMOS transistors were used in order to allow a faster read access time due to the above mentioned problem the read out circuitry is provided the supply voltage through the read enable signal in order to save substantial static power because of the leaky low voltage threshold devices the schematic diagram with the two sensing nodes of static and dynamic are shown in Fig. 4.RBL saturation during readout that slows down the charging and discharging operation as the RBL voltage increases and decreases The raising edge of the read clock (RCLK) creates a precharge pulse that charges the parasitic capacitance of RBL and discharges the dynamic sense inverter output capacitance through the discharge transistor, . Subsequently RBL is conditionally discharge during read operation turning on to complement the output if high value is stored in the selected cell. Therefore an RBL swing of only one threshold voltage is required to complete a read operation.

B. Write Circuitry

The proposed single supply 3T bit cell provide a significant improvement in write time when compared to the read time, which means it has fast access time, when compared to the readout circuitry. It also has an initial SN level improvement over standard GC implementation the dual transistor write port built by means of transmission gate provides a leakage path to or from the storage node. The write circuitry to implement the median WBL bias during standby and read cycle is shown in Fig.5.

VII. RESULTS AND DISCUSSIONS

S.No	Power Consumption		
	Various Memories	Average Power Conumption (Mw)	Data Retention Power (Nw)
1. 2. 3.	6T SRAM 2TMIXED GAIN CELL 3T GC-eDRAM	36.85 13.20 12.70	- 5.98 4.66

The functionality of the memories at different frequencies for various voltage range are shown in Fig. 7 and their corresponding power consumptions results are discussed as follows. The main aim of the proposed techniques is that 3T GC-eDRAM should consume less power than that of the other memories such as static RAM (SRAM) designed with 6 transistors and 2T mixed GC DRAM architecture 3T GC- eDRAM has a average power consumption of 12.71µW which is less when compared to other existing memories 6T SRAM and 2Tmixed GC which consumes average power of 36.85µW and 13.2µW respectively. The result shows that the proposed technology consumes very less power than that of static memory. For a dynamic memory relevant metric for static power consumption is retention power, composed of the sum of leakage and refresh power. Hence it is essential to be much more low so that the power consumption due to leakage and refreshing operation get reduced. The data retention power of 3T GC-eDRAM.

VIII. CONCLUSION

This brief proposes a novel 3T GC eDRAM microcell targeted at ULP systems and providing high storage density. The proposed GC is operated from a single-supply voltage, eliminating the need for boosted voltages, commonly found in prior-art implementations. When compared with 6T SRAM technology and 2T mixed gain cell technology it has less consumption of power and becomes fully functional at the voltage range of 600mv to 2.5v showing a worst case Data Retention power of 4.6 nW at 900mv.The proposed cell exhibits faster write-access than conventional GC circuits, thereby increasing DRTs and reducing refresh power consumption. The average power consumption at write access time is less than that of read access time. Measurement resultsshow full functionality at voltages ranging from 600 mv to 2.5 V with power as much as lower than apreviously reported 6T SRAM in the same technology node. Testing is the major issue in eDRAM technology. So in future various

testing method can be used to check the better performance of the circuit.

REFERENCES

[1]. P. Nirmala, T. Manimegalai, J. R. Arunkumar, S. Vimala, G. Vinoth Rajkumar, Raja Raju, "A Mechanism for Detecting the Intruder in the Network through a Stacking Dilated CNN Model", Wireless Communications and Mobile Computing, vol. 2022, Article ID 1955009, 13 pages, 2022. https://doi.org/10.1155/2022/1955009.

[2]. D. Sathyanarayanan, T. S. Reddy, A. Sathish, P. Geetha, J. R. Arunkumar and S. P. K. Deepak, "American Sign Language Recognition System for Numerical and Alphabets," 2023 International Conference on Research Methodologies in Knowledge Management, Artificial Intelligence and Telecommunication Engineering (RMKMATE), Chennai, India, 2023, pp. 1-6, doi: 10.1109/RMKMATE59243.2023.10369455.

[3]. J. R. Arunkumar, Tagele berihun Mengist, 2020" Developing Ethiopian Yirgacheffe Coffee Grading Model using a Deep Learning Classifier" International Journal of Innovative Technology and Exploring Engineering (IJITEE) ISSN: 2278-3075, Volume-9 Issue-4, February 2020. DOI: 10.35940/ijitee.D1823.029420.

[4]. Ashwini, S., Arunkumar, J.R., Prabu, R.T. et al. Diagnosis and multi-classification of lung diseases in CXR images using optimized deep convolutional neural network. Soft Comput (2023). https://doi.org/10.1007/s00500-023-09480-3

[5]. J.R.Arunkumar, Dr.E.Muthukumar," A Novel Method to Improve AODV Protocol for WSN" in Journal of Engineering Sciences" ISSN NO: 0377-9254Volume 3, Issue 1, Jul 2012.

[6]. R. K, A. Shameem, P. Biswas, B. T. Geetha, J. R. Arunkumar and P. K. Lakineni, "Supply Chain Management Using Blockchain: Opportunities, Challenges, and Future Directions," 2023 Second International Conference on Informatics (ICI), Noida, India, 2023, pp. 1-6, doi: 10.1109/ICI60088.2023.10421633.

[7]. Arunkumar, J. R. "Study Analysis of Cloud Security Chanllenges and Issues in Cloud Computing Technologies." Journal of Science, Computing and Engineering Research 6.8 (2023): 06-10.

[8]. J. R. Arunkumar, R. Raman, S. Sivakumar and R. Pavithra, "Wearable Devices for Patient Monitoring System using IoT," 2023 8th International Conference on Communication and Electronics Systems (ICCES), Coimbatore, India, 2023, pp. 381-385, doi: 10.1109/ICCES57224.2023.10192741.

[9]. S. Sugumaran, C. Geetha, S. S, P. C. Bharath Kumar, T. D. Subha and J. R. Arunkumar, "Energy Efficient Routing Algorithm with Mobile Sink Assistance in Wireless Sensor Networks," 2023 International Conference on Advances in Computing, Communication and Applied Informatics (ACCAI), Chennai, India, 2023, pp. 1-7, doi: 10.1109/ACCAI58221.2023.10201142.

[10]. R. S. Vignesh, V. Chinnammal, Gururaj.D, A. K. Kumar, K. V. Karthikeyan and J. R. Arunkumar, "Secured Data Access and Control Abilities Management over Cloud Environment using Novel Cryptographic Principles," 2023 International Conference on Advances in Computing, Communication and Applied Informatics (ACCAI), Chennai, India, 2023, pp. 1-8, doi: 10.1109/ACCAI58221.2023.10199616.

[11]. Syamala, M., Anusuya, R., Sonkar, S.K. et al. Big data analytics for dynamic network slicing in 5G and beyond with dynamic user preferences. Opt Quant Electron 56, 61 (2024). https://doi.org/10.1007/s11082-023-05663-2

[12]. Krishna Veni, S. R., and R. Anusuya. "Design and Study Analysis Automated Recognition system of Fake Currency Notes." Journal of Science, Computing and Engineering Research 6.6 (2023): 16-20.

[13]. V. RamKumar, S. Shanthi, K. S. Kumar, S. Kanageswari, S. Mahalakshmi and R. Anusuya, "Internet of Things Assisted Remote Health and Safety Monitoring Scheme Using Intelligent Sensors," 2023 International Conference on Advances in Computing, Communication and Applied Informatics (ACCAI), Chennai, India, 2023, pp. 1-8, doi: 10.1109/ACCAI58221.2023.10199766.

[14]. R. S. Vignesh, R. Sankar, A. Balaji, K. S. Kumar, V. Sharmila Bhargavi and R. Anusuya, "IoT Assisted Drunk and Drive People Identification to Avoid Accidents and Ensure Road Safety Measures," 2023 International Conference on Advances in Computing, Communication and Applied Informatics (ACCAI), Chennai, India, 2023, pp. 1-7, doi: 10.1109/ACCAI58221.2023.10200809.

[15]. I. Chandra, G. Sowmiya, G. Charulatha, S. D, S. Gomathi and R. Anusuya, "An efficient Intelligent Systems for Low-Power Consumption Zigbee-Based Wearable Device for Voice Data Transmission," 2023 International Conference on Artificial Intelligence and Knowledge Discovery in Concurrent Engineering (ICECONF), Chennai, India, 2023, pp. 1-7, doi: 10.1109/ICECONF57129.2023.10083856.

[16]. G. Karthikeyan, D. T. G, R. Anusuya, K. K. G, J. T and R. T. Prabu, "Real-Time Sidewalk Crack Identification and Classification based on Convolutional Neural Network using Thermal Images," 2022 International Conference on Automation, Computing and Renewable Systems (ICACRS), Pudukkottai, India, 2022, pp. 1266-1274, doi: 10.1109/ICACRS55517.2022.10029202.

[17]. R. Meena, T. Kavitha, A. K. S, D. M. Mathew, R. Anusuya and G. Karthik, "Extracting Behavioral Characteristics of College Students Using Data Mining on Big Data," 2023 International Conference on Artificial Intelligence and Knowledge Discovery in Concurrent Engineering (ICECONF), Chennai, India, 2023, pp. 1-7, doi: 10.1109/ICECONF57129.2023.10084276.

[18]. S. Bharathi, A. Balaji, D. Irene. J, C. Kalaivanan and R. Anusuya, "An Efficient Liver Disease Prediction based on Deep Convolutional Neural Network using Biopsy Images," 2022 3rd International Conference on Smart Electronics and Communication (ICOSEC), Trichy, India, 2022, pp. 1141-1147, doi: 10.1109/ICOSEC54921.2022.9951870.

[19]. I. Chandra, G. Sowmiya, G. Charulatha, S. D, S. Gomathi and R. Anusuya, "An efficient Intelligent Systems for Low-Power Consumption Zigbee-Based Wearable Device for Voice Data Transmission," 2023 International Conference on Artificial Intelligence and Knowledge Discovery in Concurrent Engineering (ICECONF), Chennai, India, 2023, pp. 1-7, doi: 10.1109/ICECONF57129.2023.10083856.

[20]. Revathi, S., et al. "Developing an Infant Monitoring System using IoT (INMOS)." International Scientific Journal of Contemporary Research in Engineering Science and Management 6.1 (2021): 111-115.