Journal of Science, Computing and Engineering Research (JSCER)
Volume-8, Issue- 8, August 2024.
DOI: *https://doi.org/10.46379/jscer.2023.070401*
ISSN: 2708-1079

A case study of Insurance Companies Quality Leadership Style in Relation to Enterprise Commitment in India

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Article Information

Received : 02 August 2025
Revised : 06 August 2025
Accepted : 08 August 2025
Published : 10 August 2025

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Abstract— This paper presents the comparison of proposed double tail comparator with conventional double tail and existing double tail comparator. The low power and high-speed analog to digital converters used are of dynamic regenerative comparators to maximize speed. Presenting different architectures for calculating delay and power consumption in dynamic double tail comparator. The power gating technique is used to design the proposed comparator. By using this technique, delay and power consumption is reduced compared to the conventional double tail comparator and the existing double tail comparator. The important parameters are speed and power consumption. Cadence design tools used to simulate the comparator in the 90nm technology with the supply voltage of 0.6v.

Keywords: ***Dynamic latch comparator, speed, power consumption, high speed analog to digital converter.***

Citation: Grihidhar Menon, Nivitha D, "A case study of Insurance Companies Quality Leadership Style in Relation to Enterprise Commitment in India", Journal of Science, Computing and Engineering Research, 8(8),2025.

I. INTRODUCTION

Comparator is a circuit that output is binary information depending upon the comparison of two input voltages here the comparison in between analog voltage and reference voltage. Analog voltage is greater than reference voltage, and then comparator output is logic '1'. The comparator output is logic '0', when analog voltage is less than reference voltage. Comparators are effectively used in analog to digital (ADC) converters. In analog to digital conversion process [1], the analog voltage is converted in to samples for getting accuracy. Those samples are given to set of comparators in order to achieve equivalent binary information. The schematic of a voltage comparator shown in Fig 1.Comparator transfer characteristics shown in Fig 2. Comparator truth table shown in Table 1. Comparator applications are analog to digital converters and data receivers. The dynamic latch comparators used in these applications in order to achieve high-speed and low power. Dynamic comparators have no static power consumption because of strong positive feedback. Dynamic latch comparator [3] is suitable for high-speed analog to digital converters (ADC). The first stage of clocked comparator is given to the inputs. Second stage of clocked comparator consists of two cross coupled inverters called regenerative stage. In this stage each inverter input is connected to the other inverter output. The important parameters like speed, power consumption, and transistor count are very important in comparator applications. By using a clocked regenerative structure will get low power and good output swing. When the clock is high (CLK= VDD) comparator circuit works in comparison phase. When the clock is low (CLK=0)

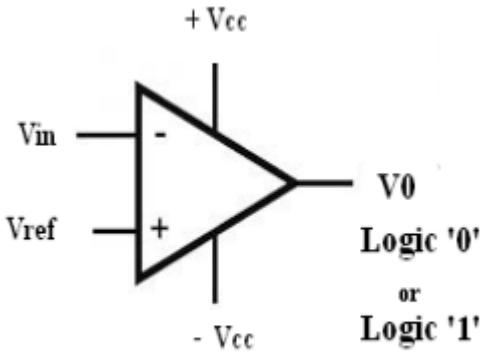

Fig 1. Schematic of comparator

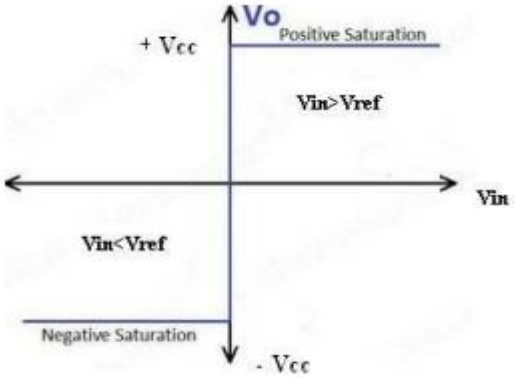

Fig 2. Comparator Transfer Characteristics

TABLE 1.
COMPARATOR TRUTH TABLE

CLK	INN	INP	OUTN	OUTP
0	X	X	1	1
1	0	0	0	0
1	0	1	1	0
1	1	0	0	1
1	1	1	0	0

suffers from low supply voltages for designing high speed comparators. Hence, designing highspeed comparators with low supply voltages many techniques are there such boosting [6] methods, techniques employing body driven comparator circuit works in reset phase. CMOS technology

II. RELATED WORKS

In comparator circuits to reduce power consumption the Power gating technique is proposed. In this technique, circuit operates in sleep mode by switching off the current in circuit. Power gating has the benefit that is it measures current (Idd) in the quiescent state. In this paper the different architectures of double tail comparator is presented. The proposed comparator is designed by using power gating technique. Using this technique power and delay is reduced.

III. BACKGROUND OF STUDY

The circuit diagram of the single tail comparator shown in Fig 3. The single tail comparator circuit operation is given below. When CLK=0 the circuit works in reset phase so the Mtail NMOS transistor is in off position and the reset transistors M7 and M8 PMOS transistors are in on position now the output at OUTN and OUTP will be VDD. When CLK= VDD , Mtail NMOS transistor is in ON position and M7 and M8 PMOS transistors are in OFF position now the OUTN and OUTP output nodes are discharge depending on the INN and INP input voltages. When INP>INN, M5 PMOS transistor will turn ON because of OUTP discharges more speed than OUTN then the output at OUTN= VDD and output at OUTP=0. When INP INN voltage, drain current of the transistor M2 causes faster discharge of OUTP compared to OUTN. Advantages of the single tail comparator are high input impedance, output swing without noise, no static power consumption. The disadvantage is only one current path is available via Mtail NMOS transistor which defines the current for both the differential amplifiers that means a small tail current to keep the differential amplifiers in weak condition so a large current required enabling fast regeneration in the circuit.

IV. METHODOLOGY

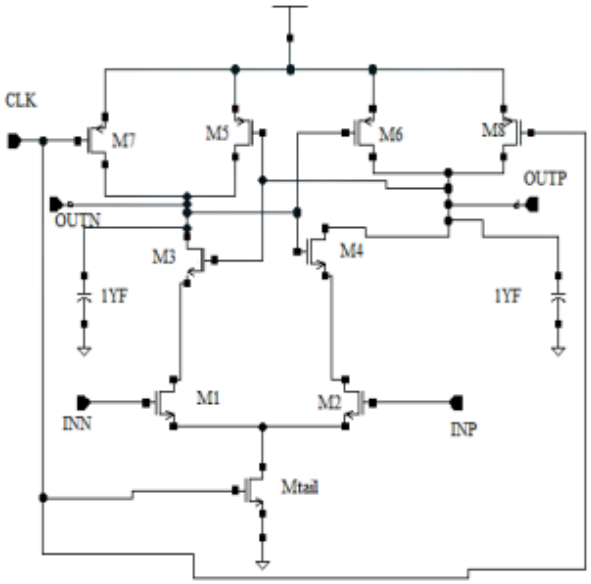

Fig 3. Circuit diagram of the single tail comparator

This structure has the power consumption 20.49 nW and circuit delay is 38.83 ps. Circuit diagram of the conventional double tail comparator shown in Fig 4. This structure has low static power consumption and operates at lower supply voltages compare to the single tail comparator. The working of this comparator is given below.

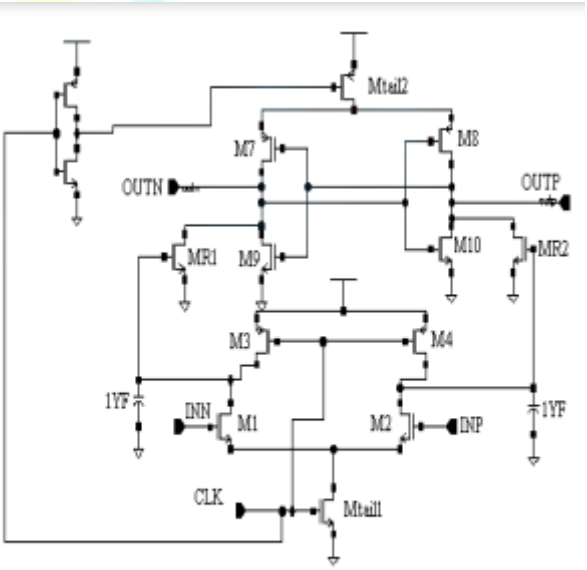

Fig 4. Circuit diagram of conventional Double tail comparator

When CLK=0 the circuit works in reset phase so the Mtail1 NMOS transistor and Mtail2 PMOS transistor are in OFF position and the M3 and M4 PMOS transistors will turn on then the value at nodes fn and fp= VDD due to this VDD, MR1 and MR2 turn ON and discharge the output nodes OUTP and OUTN to the ground. When CLK= VDD,

the circuit works in comparison phase resulting in Mtail1 NMOS transistor and Mtail2 PMOS transistor to switch ON. The M3 and M4 PMOS transistors will turn OFF then the voltages at nodes fn and fp starts to discharge with different charging rates. Due to these discharging transistors MR1 and MR2 are in OFF position so they do not play any role in improving the transconductance. The circuit power consumption and delay is 59.06 nW and 80.09 ns respectively. The IV section explains how the existing comparator improves performance of double tail comparator.

Circuit diagram of the existing double tail comparator with static power consumption shown in Fig 5. The existing comparator designed for low voltage applications based on conventional double tail comparator. The main idea of this comparator is to increase Vfn/Vfp ratio and speed up the latch regenerative circuit. MC1 and MC2 PMOS control transistors are connected in parallel to M3 and M4 PMOS transistors. This set up is used to increase speed of the existing comparator. Power consumption of this comparator is 3.468 uW and over all delay is 20.31 ns. The schematic of existing double tail comparator without static power consumption shown in Fig 6. The working of proposed double tail comparator is given below.

When CLK=0 the circuit works in reset phase, Mtail1 NMOS transistor and Mtail2 PMOS transistor are in OFF position and the M3 and M4 PMOS transistors will turn ON then the value at nodes fn and fp= VDD, hence MC1 and MC2 PMOS transistors are OFF. Intermediate stage transistors MR1 and MR2 will turn ON because of the value at nodes fn and fp= VDD. Consequently the value at OUTN and OUTP=0. When CLK=VDD the circuit works in comparison phase so the Mtail1 NMOS transistor and Mtail2 PMOS transistor is in ON position and the transistors M3 and M4 are in OFF state, nodes fn and fp start to discharge at different charging rates depending on the input voltages INN and INP. When INP voltage>INN voltage, M1 NMOS transistor provides less current than M2 NMOS transistor due to this current fn discharges faster than fp. The disadvantage of this structure is static power consumption whenever the current drawn from VDD to ground through input and Mtail1 transistor. To overcome static power consumption in proposed double tail comparator two NMOS transistors MSW1 and MSW2 used below the input transistor

V. RESULTS AND DISCUSSIONS

All the circuits are designed by using Cadence Virtuoso tool and simulated in 90 nm CMOS technology with the supply voltage of 0.6V. The output waveform of comparator shown in Fig 8. Power waveform of the single tail comparator is shown in Fig 9. Conventional double tail comparator's power waveform shown in Fig 10. Power waveforms of the existing double tail with static power and without static power are shown in Fig 11 and Fig 12 respectively. Power waveform of the proposed double tail comparator shown in Fig13. Power comparison and delay comparison shown in Table 2 and Table 3 respectively. From this analysis known that the proposed double tail comparator consumed less power and delay also reduced compare to existing and conventional double tail comparator.

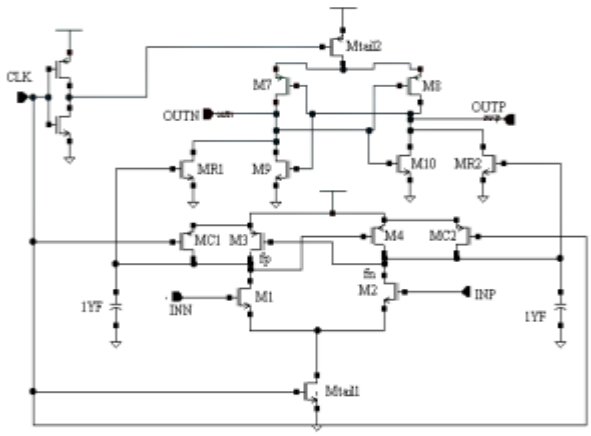

Fig 5. Schematic of the existing Double tail comparator with static power consumption

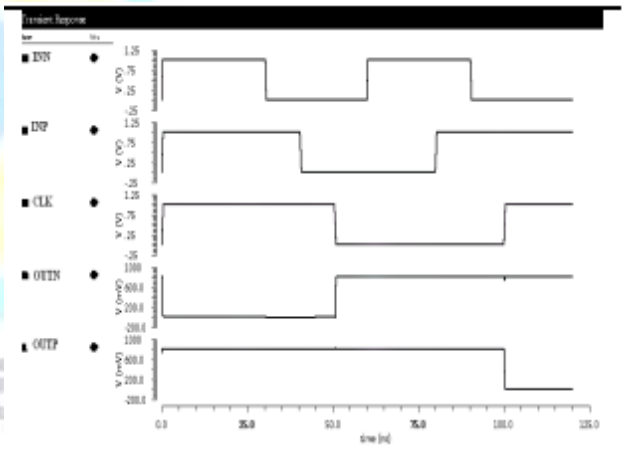

Fig 8. Output waveform of comparator

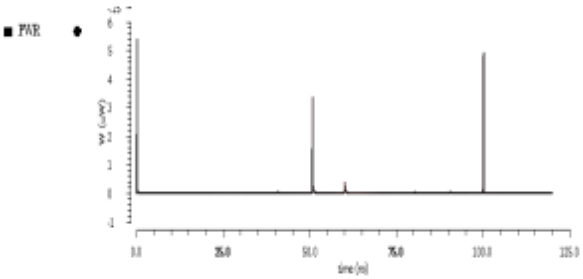

Fig 9. Power waveform of the single tail comparator

VI. CONCLUSION

Comparison of three double tail comparator circuits being done. All the circuits simulated by using cadence design

tools 90nm technology with the supply voltage of 0.6 volt. Using the power gating technique, power consumption and delay is reduced in the proposed double tail comparator. The proposed double tail comparator consumes less power and delay is also reduced compare to previous comparator circuits. Due to additional NMOS transistors there is an increase in area. The comparator circuit used in analog to digital converter structures, sense amplifier, operational amplifier and pre defined amplifier.

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